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ACCELERATED LIFE TESTING EFFECTS ON CMOS MICROCIRCUIT CHARACTERISTICS

By RCA, Inc.
Solid State Division
Somerville, New Jersey

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Final Report

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SECTION I

INTRODUCTION

The need for a practical short-term test program, the results of which can be meaningfully interpreted to predict the long-term reliability of CMOS microcircuits, has been recognized. Many months if not years are required to run a life test under conditions reflecting actual applications and requirements of Class A devices. The impracticality of such a test led to the reliance by the industry on long-term reliability predictions based on interpolations of results gathered from accelerated life tests. It is essential to run long (thousands of hours) 125°C life tests to corfirm experimentally the validity of such interpolations for CMOS devices. There is a definite possibility that accelerated tests cause the temperature thresholds of a device to be exceeded, thus triggering failure mechanisms unrelated to a device's operation within its specified ratings. The somewhat arbitrary limits established for the use of accelerated life tests must be either experimentally confirmed or revised in accordance with experimental data. The varying complexity of present day CMOS devices should be recognized as a factor in reliability predictions.

SECTION II

OBJECTIVE

The purpose of this program is to determine the consistency of the CMOS microcircuit activation energy in the range of 125°C to 200°C and 200°C to 250°C. Also, this program will determine the relationship of accelerated life-test failures to rated temperature operation and provide a basis for recommendations for accelerated life tests within the scope of the M38510 specifications.

The program encompasses three phases. Phase I is the 250°C accelerated life test, Phase II is the 200°C accelerated life test, and Phase III is the 125°C accelerated life test. In Phases I and II, the objective is to conduct a life test of sufficient duration to generate a minimum of 50 percent cumulative failures. In Phase III, the life test is conducted for 20,000 hours. The collected data is used a) to provide a basis for recommendations of conditions and limits to be used as part of a microcircuit qualification procedure, b) to determine whether any thresholds that could trigger failure mechanisms unique to that temperature are exceeded during the high-temperature testing, c) to assess the usefulness of the 250°C accelerated test as a predictor of long-term reliability.

SECTION III

DEVICE SELECTION

The choice of microcircuit devices for this program was made according to the following criteria:

1. High-reliability Class A devices.
2. Varying degree of complexity representing the product line.
3. Availability.

The following microcircuit types were chosen for this program:

MIL DESIGNATIONS	GENERIC NAMES	FUNCTION
M38510/05001ADX	CD4011A	Two-input quadruple logic NAND gate
M38510/05101ADX	CD4013A	"D"-type flip-flop
M38510/05605ADX	CD4024A	Seven-stage binary counter.

The devices are in flat packs with weldable leads. Solder-dipped leads could not be used at temperatures above the solder melting point. These devices were tested to the individual M38510/50 specifications. Table III of these specifications is attached to this report as Table I (CD4011A), Table II (CD4013A), and Table III (CD4024A). The table specifies the test conditions and limits of the electrical parameters for the group A testing for individual microcircuits. Subgroups 1,2,3,7, and 8 were performed at each measurement point throughout the test program and are the basis for the subsequent data analysis. The CD4011A was tested for functionality under conditions similar to those specified in subgroups 7 and 8 for the other two types.

Further detailed descriptions of these microcircuits are given in Figs. 1 through 7. The figures include photographs of chips with dimensions

shown, magnified photographs with detail visibility, logic diagrams, and circuit diagrams to provide a basis for comparison of the chip sizes and the complexities of the microcircuits involved. Table IV summarizes some of the complexity factors for each microcircuit type.

TABLE III. Group A inspection for device type 01.
Terminal conditions (pins not designated are open)

Symbol	MIL-STD-883 Method	Case All / Test No.	1 (1A)	2 (1B)	3 (1Y)	4 (2Y)	5 (2B)	6 (2A)	7 (V_{SS})	8 (3A)	9 (3B)	10 (3Y)	11 (4Y)	12 (4B)	13 (4A)	14 (V_{DD})	Measured terminal	Subgroup 1 T_A = 25°C Min	Subgroup 1 T_A = 25°C Max	Subgroup 2 T_A = 125°C Min	Subgroup 2 T_A = 125°C Max	Subgroup 3 T_A = -55°C Min	Subgroup 3 T_A = -55°C Max	Unit
V_{IC} (POS)		1	1 mA													GND	1A		1.5					Vdc
		2		1 mA													1B							
		3					1 mA										2B							
		4						1 mA									2A							
		5								1 mA							3A							
		6									1 mA						3B							
		7												1 mA			4B							
		8													1 mA		4A							
V_{IC} (NEG)		9	-1 mA						GND								1A		-6.0					Vdc
		10		-1 mA													1B							
		11					-1 mA										2B							
		12						-1 mA									2A							
		13								-1 mA							3A							
		14									-1 mA						3B							
		15												-1 mA			4B							
		16													-1 mA		4A							
I_{SS}	3005	17	GND	15.0 V			15.0 V	GND	GND	GND	15.0 V			15.0 V	GND	15.0 V	V_{SS}		-25.0		-750			nA
		18	15.0 V	15.0 V			15.0 V	15.0 V		15.0 V	15.0 V			15.0 V	15.0 V									
		19	15.0 V	GND			GND	15.0 V		15.0 V	GND			GND	15.0 V									
V_{OH1}	3006	20	V_{IL1}	5.0 V	I_{OH1}		GND	GND	GND	GND	GND			GND	GND	5.0 V	1Y	4.2		4.2		4.2		Vdc
		21	5.0 V	V_{IL1}	I_{OH1}		GND	GND									1Y							
		22	GND	GND		I_{OH1}	V_{IL1}	5.0 V									2Y							
		23				I_{OH1}	5.0 V	V_{IL1}									2Y							
		24					GND	GND		V_{IL1}	5.0 V	I_{OH1}					3Y							
		25								5.0 V	V_{IL1}	I_{OH1}					3Y							
		26								GND	GND		I_{OH1}	V_{IL1}	5.0 V		4Y							
		27								GND	GND		I_{OH1}	5.0 V	V_{IL1}		4Y							
V_{OH2}	3006	28	V_{IL1}	5.0 V			GND	GND	GND	GND	GND			GND	GND	5.0 V	1Y	4.95		4.95		4.95		Vdc
		29	5.0 V	V_{IL1}			GND	GND									1Y							
		30	GND	GND			V_{IL1}	5.0 V									2Y							
		31					5.0 V	V_{IL1}									2Y							
		32					GND	GND		V_{IL1}	5.0 V						3Y							
		33								5.0 V	V_{IL1}						3Y							
		34								GND	GND			V_{IL1}	5.0 V		4Y							
		35								GND	GND			5.0 V	V_{IL1}		4Y							
V_{OH3}	3006	36	V_{IL2}	12.5 V			GND	GND	GND	GND	GND			GND	GND	12.5 V	1Y	11.25		11.25		11.25		Vdc
		37	12.5 V	V_{IL2}			GND	GND									1Y							
		38	GND	GND			V_{IL2}	12.5 V									2Y							
		39	GND	GND			12.5 V	V_{IL2}									2Y							

TABLE I - Device: CD4011A, Electrical Test Parameters

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TABLE III. Group A inspection for device type 01 (cont.).
Terminal conditions (pins not designated are open)

Symbol	MIL-STD-883 Method	Case All: Symbol / Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Subgroup 1 $T_A = 25°C$ Min	Max	Subgroup 2 $T_A = 125°C$ Min	Max	Subgroup 3 $T_A = -55°C$ Min	Max	Unit
		Symbol	1A	1B	1Y	2Y	2B	2A	V_{SS}	3A	3B	3Y	4Y	4B	4A	V_{DD}								
V_{OH}	3006	40 41 42 43	GND	GND			GND	GND	GND	V_{IL2} 12.5 V GND GND	12.5 V V_{IL2} GND GND			GND GND V_{IL2} 12.5 V	GND GND 12.5 V V_{IL2}	12.5 V	3Y 3Y 4Y 4Y	11.25		11.25		11.25		Vdc
V_{OL1}	3007	44 45 46 47	V_{IH1} GND	V_{IH1} GND	I_{OL1}	I_{OL1}	GND V_{IH1} GND GND	GND V_{IH1} GND GND	GND	GND GND V_{IH1} GND	GND GND V_{IH1} GND	I_{OL1}	I_{OL1}	GND V_{IH1}	GND V_{IH1}	5.0 V	1Y 2Y 3Y 4Y		0.5		0.5		0.5	Vdc
V_{OL2}	3007	48 49 50 51	V_{IH1} GND	V_{IH1} GND			GND V_{IH1} GND GND	GND V_{IH1} GND GND	GND	GND GND V_{IH1} GND	GND GND V_{IH1} GND			GND V_{IH1}	GND V_{IH1}	5.0 V	1Y 2Y 3Y 4Y		0.05		0.05		0.05	Vdc
V_{OL3}	3007	52 53 54 55	V_{IH2} GND GND GND	V_{IH2} GND GND GND			GND V_{IH2} GND GND	GND V_{IH2} GND GND	GND GND GND GND	GND GND V_{IH2} GND	GND GND V_{IH2} GND			GND GND GND V_{IH2}	GND GND GND V_{IH2}	12.5 V 12.5 V 12.5 V 12.5 V	1Y 2Y 3Y 4Y		1.25		1.25		1.25	Vdc
I_{IH1} 1/	3010	56	15.0 V	15.0 V			15.0 V	15.0 V	GND	15.0 V	15.0 V			15.0 V	15.0 V	15.0 V	All together		8.0					nA
I_{IH2}	3010	57 58 59 60 61 62 63 64	15.0 V	15.0 V			15.0 V	15.0 V	GND	15.0 V	15.0 V			15.0 V	15.0 V	15.0 V	1A 1B 2B 2A 3A 3B 4B 4A		1.0		45.0			nA
I_{IL1} 1/	3009	65	GND	GND			GND	GND	GND	GND	GND			GND	GND	15.0 V	All together		-8.0					nA
I_{IL2}	3009	66 67 68 69 70 71 72 73	GND 15.0 V	15.0 V GND 15.0 V			15.0 V 15.0 V GND 15.0 V	15.0 V 15.0 V 15.0 V GND 15.0 V	GND	15.0 V 15.0 V GND 15.0 V 15.0 V 16.0 V	15.0 V 15.0 V GND 15.0 V 15.0 V			15.0 V 15.0 V GND 15.0 V	15.0 V 15.0 V GND	15.0 V	1A 1B 2B 2A 3A 3B 4B 4A		-1.0		-45.0			nA

See footnote at end of table III for device type 03.

TABLE I - Device: CD4011A, Electrical Test Parameters, (continued)

TABLE III. Group A inspection for device type 01 (cont.).
Terminal conditions (pins not designated are open)

Symbol	MIL-STD-883 Method	Case All: Test No.	1 1A	2 1B	3 1Y	4 2Y	5 2B	6 2A	7 V_{SS}	8 3A	9 3B	10 3Y	11 4Y	12 4B	13 4A	14 V_{DD}	Measured terminal	Test limits: Min	Max	Min	Max	Min	Max	Unit
																		Subgroup 4 T_A = 25°C						
C_I	3012	74 75 76 77 78 79 80 81	F	F			F	F	GND	F	F			F	F	GND	1A 1B 2B 2A 3A 3B 4B 4A		12.0					pF
																		Subgroup 9 T_A = 25°C		Subgroup 10 T_A = 125°C		Subgroup 11 T_A = -55°C		
t_{PHL}	3003 Fig. 7	82 83 84 85 86 87 88 89	IN 5.0 V	5.0 V IN 5.0 V	OUT OUT	OUT OUT	5.0 V 5.0 V IN 5.0 V	5.0 V IN 5.0 V	GND	5.0 V IN 5.0 V	5.0 V IN 5.0 V 5.0 V	OUT OUT	OUT OUT	5.0 V IN 5.0 V	5.0 V IN	5.0 V	1A to 1Y 1B to 1Y 2A to 2Y 2B to 2Y 3A to 3Y 3B to 3Y 4A to 4Y 4B to 4Y	20	200	30	300	15	200	ns
t_{PLH}	3003 Fig. 7	90 91 92 93 94 95 96 97	IN 5.0 V	5.0 V IN 5.0 V	OUT OUT	OUT OUT	5.0 V 5.0 V IN 5.0 V	5.0 V IN 5.0 V	GND	5.0 V IN 5.0 V	5.0 V IN 5.0 V 5.0 V	OUT OUT	OUT OUT	5.0 V IN 5.0 V	5.0 V IN	5.0 V	1A to 1Y 1B to 1Y 2A to 2Y 2B to 2Y 3A to 3Y 3B to 3Y 4A to 4Y 4B to 4Y	20	150	30	225	15	150	ns
T_{THL}	3004 Fig. 7	98 99 100 101 102 103 104 105	IN 5.0 V	5.0 V IN 5.0 V	OUT OUT	OUT OUT	5.0 V 5.0 V IN 5.0 V	5.0 V IN 5.0 V	GND	5.0 V IN 5.0 V	5.0 V IN 5.0 V 5.0 V	OUT OUT	OUT OUT	5.0 V IN 5.0 V	5.0 V IN	5.0 V	1Y 1Y 2Y 2Y 3Y 3Y 4Y 4Y	30	300	45	450	25	300	ns
T_{TLH}	3004 Fig. 7	106 107 108 109 110 111 112 113	IN 5.0 V	5.0 V IN 5.0 V	OUT OUT	OUT OUT	5.0 V 5.0 V IN 5.0 V	5.0 V IN 5.0 V	GND	5.0 V IN 5.0 V	5.0 V IN 5.0 V 5.0 V	OUT OUT	OUT OUT	5.0 V IN 5.0 V	5.0 V IN	5.0 V	1Y 1Y 2Y 2Y 3Y 3Y 4Y 4Y	40	300	60	450	30	300	ns

TABLE I - Device: CD4011A, Electrical Test Parameters, (continued)

TABLE III Group A inspection for device type 01

Symbol	MIL-STD-883 method	Cases C, D	Terminal conditions and limits														Measured terminal	Test limits						Units
		Symbol	Q_1	$\overline{Q_1}$	CLK_1	RS_1	D_1	SET_1	V_{SS}	SET_2	D_2	RS_2	CLK_2	$\overline{Q_2}$	Q_2	V_{DD}		Subgroup 1 $T_A = 25°C$		Subgroup 2 $T_A = 125°C$				
		Test No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	Min	Max	Min	Max	
$V_{IC(pos)}$		1						1 mA								GND	Set 1		1.5					Vdc
		2				1 mA											RS_1							
		3					1 mA										D_1							
		4			1 mA												CLK_1							
		5								1 mA							SET_2							
		6										1 mA					RS_2							
		7									1 mA						D_2							
		8											1 mA				CLK_2							
$V_{IC(neg)}$		9						-1 mA	GND								Set_1		-8					
		10				-1 mA											RS_1							
		11					-1 mA										D_1							
		12			-1 mA												CLK_1							
		13								-1 mA							SET_2							
		14										-1 mA					RS_2							
		15									-1 mA						D_2							
		16											-1 mA				CLK_2							
I_{SS} See note B	3005	17			15 V	GND	GND	GND	GND	GND	GND	GND	GND			15 V	None		25		-2			µA
		18			GND		GND										None							
		19			15 V		GND										None							
		20			15 V		15 V										V_{SS}							
		21			GND		15 V										V_{SS}							
		22			15 V		15 V										None							
		23			15 V		GND										None							
		24			GND		GND										V_{SS}							
		25			15 V	GND	GND										None							
		26			15 V	15 V	15 V	15 V									V_{SS}							
		27			GND	15 V	15 V	15 V									V_{SS}							
		28			GND	GND	GND	GND					15 V				None							
		29											GND				None							
		30											15 V				None							
		31									15 V		15 V				V_{SS}							
		32									15 V		GND				V_{SS}							
		33									15 V		15 V				None							
		34									GND		15 V				None							
		35									GND		GND				V_{SS}							
		36									GND		15 V				None							
		37								15 V	15 V	15 V	15 V				V_{SS}							
		38								15 V	15 V	15 V	GND				V_{SS}							

TABLE II - Device: CD4013A, Electrical Test Parameters

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TABLE III. Group A inspection for device type 01 - Continued

Symbol	MIL-STD-883 method	Cases C, D	Terminal conditions and limits														Measured terminal	Test limits						Units
		Symbol	Q_1	$\bar{Q}_1$	CLK_1	RS_1	D_1	SET_1	V_{SS}	SET_2	D_2	RS_2	CLK_2	$\bar{Q}_2$	Q_2	V_{DD}		Subgroup 1 $T_A = 25°C$		Subgroup 2 $T_A = 125°C$		Subgroup 3 $T_A = -55°C$		
		Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14		Min	Max	Min	Max	Min	Max	
V_{OH1}	3006	39	I_{OH}		GND	V_{IL1}	GND	V_{IH1}	GND	GND	GND	GND	GND			5.0 V	Q_1	4.5		4.5		4.5		Vdc
		40		I_{OH}		V_{IH1}		V_{IL1}		GND		GND					$\bar{Q}_1$							
		41				GND		GND		V_{IH1}		V_{IL1}			I_{OH}		Q_2							
		42				GND		GND		V_{IL1}		V_{IH1}		I_{OH}			$\bar{Q}_2$							
V_{OH2}		43				V_{IL1}		V_{IH1}		GND		GND					Q_1	4.95		4.95		4.95		
		44				V_{IH1}		V_{IL1}		GND		GND					$\bar{Q}_1$							
		45				GND		GND		V_{IH1}		V_{IL1}					Q_2							
		46				GND		GND		V_{IL1}		V_{IH1}					$\bar{Q}_2$							
V_{OH3}		47				V_{IL2}		V_{IH2}		GND		GND				12.5 V	Q_1	11.25		11.25		11.25		
		48				V_{IH2}		V_{IL2}		GND		GND					$\bar{Q}_1$							
		49				GND		GND		V_{IH2}		V_{IL2}					Q_2							
		50				GND		GND		V_{IL2}		V_{IH2}					$\bar{Q}_2$							
V_{OL1}	3007	51	I_{OL}			V_{IH1}		V_{IL1}		GND		GND				5.0 V	Q_1		0.5		0.5		0.5	
		52		I_{OL}		V_{IL1}		V_{IH1}		GND		GND					$\bar{Q}_1$							
		53				GND		GND		V_{IL1}		V_{IH1}			I_{OL}		Q_2							
		54				GND		GND		V_{IH1}		V_{IL1}		I_{OL}			$\bar{Q}_2$							
V_{OL2}		55				V_{IH1}		V_{IL1}		GND		GND					Q_1		0.5		0.5		0.5	
		56				V_{IL1}		V_{IH1}		GND		GND					$\bar{Q}_1$							
		57				GND		GND		V_{IL1}		V_{IH1}					Q_2							
		58				GND		GND		V_{IH1}		V_{IL1}					$\bar{Q}_2$							
V_{OL3}		59				V_{IH2}		V_{IL2}		GND		GND				12.5 V	Q_1		1.25		1.25		1.25	
		60				V_{IL2}		V_{IH2}		GND		GND					$\bar{Q}_1$							
		61				GND		GND		V_{IL2}		V_{IH2}					Q_2							
		62				GND		GND		V_{IH2}		V_{IL2}					$\bar{Q}_2$							
V_{OH4}		63			I	GND	V_{IL1}	I		GND		GND				5.0 V	Q_1	4.95		4.95		4.95		
V_{OL4}		64			I		V_{IL1}	I		GND							$\bar{Q}_1$		0.05		0.05		0.05	
V_{OH4}		65			GND		GND	GND		I	V_{IL1}		I				Q_2	4.95		4.95		4.95		
V_{OL4}		66			GND		GND	GND		I	V_{IL1}		I				$\bar{Q}_2$		0.05		0.05		0.05	
V_{OL4}		67			I		V_{IH1}	I		GND	GND		GND				Q_1		0.05		0.05		0.05	
V_{OH4}		68			I		V_{IH1}	I		GND	GND		GND				$\bar{Q}_1$	4.95		4.95		4.95		
V_{OL4}		69			GND		GND	GND		I	V_{IH1}		I				Q_2		0.05		0.05		0.05	
V_{OH4}		70			GND		GND	GND		I	V_{IH1}		I				$\bar{Q}_2$	4.95		4.95		4.95		
V_{ICL1}		71			J		J	J		GND	GND		GND				CLK_1, J	V_{IL1}	V_{IH1}	V_{IL1}	V_{IH1}	V_{IL1}	V_{IH1}	
V_{ICL1}		72			J		J	J		GND	GND		GND				CLK_1, J							
V_{ICL2}		73			GND		GND	GND		J	J		J				CLK_2, J	V_{IL1}	V_{IH1}	V_{IL1}	V_{IH1}	V_{IL1}	V_{IH1}	
V_{ICL2}		74			GND		GND	GND		J	J		J				CLK_2, J							

<u>TABLE II - Device: CD4013A, Electrical Test Parameters, (continued)</u>

TABLE III. Group A inspection for device type 01 - Continued.

Symbol	MIL-STD-883 method	Cases C, D Symbol / Test No	Terminal conditions and limits: Q_1 1	$\bar{Q}_1$ 2	CLK_1 3	RS_1 4	D_1 5	SET_1 6	V_{SS} 7	SET_2 8	D_2 9	RS_2 10	CLK_2 11	$\bar{Q}_2$ 12	Q_2 13	V_{DD} 14	Measured terminal	Test limits: Subgroup 1 $T_A = 25°C$ Min	Subgroup 1 $T_A = 25°C$ Max	Subgroup 2 $T_A = 125°C$ Min	Subgroup 2 $T_A = 125°C$ Max	Subgroup 3 $T_A = -55°C$ Min	Subgroup 3 $T_A = -55°C$ Max	Units
I_{IH1} See note K	3010	75			15 V	15 V	15 V	15 V	GND	15 V	15 V	15 V	15 V			15 V	All inputs together		8					nA
I_{IH2}		76															CLK_1		1.0		45			
		77															RS_1							
		78															D_1							
		79															SET_1							
		80															SET_2							
		81															D_2							
		82															RS_2							
		83															CLK_2							
I_{IL1} See note K	3009	84			GND	GND	GND	GND		GND	GND	GND	GND				All inputs together		-8.0					
I_{IL2}		85															CLK_1		-1.0		-45			
		86															RS_1							
		87															D_1							
		88															SET_1							
		89															SET_2							
		90															D_2							
		91															RS_2							
		92															CLK_2							
																		Subgroup 4 $T_A = 25°C$						
C_I	3012	93			L				GND							GND	CLK_1		12					pF
		94				L											RS_1							
		95					L										D_1							
		96						L									SET_1							
		97								L							SET_2							
		98									L						D_2							
		99										L					RS_2							
		100											L				CLK_2							

TABLE II - Device: CD4013A, Electrical Test Parameters, (continued)

TABLE III Group A inspection for device type 01 -Continued.

Symbol	MIL-STD-883 method	Cases C, D Symbol / Test No.	Q_1 (1)	$\bar{Q}_1$ (2)	CLK_1 (3)	RS_1 (4)	D_1 (5)	SET_1 (6)	V_{SS} (7)	SET_2 (8)	D_2 (9)	RS_2 (10)	CLK_2 (11)	$\bar{Q}_2$ (12)	Q_2 (13)	V_{DD} (14)	Measured terminal	Subgroup 7 $T_A = 25°C$ Min	Subgroup 7 $T_A = 25°C$ Max	Subgroup 8 $T_A = 125°C$ Min	Subgroup 8 $T_A = 125°C$ Max	Subgroup 8 $T_A = -55°C$ Min	Subgroup 8 $T_A = -55°C$ Max	Units
Truth table test	3014	101			5 0 V	GND	GND	GND	GND	GND	GND	GND	5 0 V			5 0 V	None			See notes M and N				
		102			GND		GND				GND		GND				None							
		103	L	H	5 0 V		GND				GND		5 0 V	H	L		All outputs							
		104	L	H	5 0 V		5 0 V				5 0 V		5 0 V	H	L									
		105	L	H	GND								GND	H	L									
		106	H	L	5 0 V								5 0 V	L	H									
		107	L	H	5 0 V	5.0 V						5 0 V	5 0 V	H	L									
		108	L	H	GND	5 0 V						5 0 V	GND	H	L									
		109	L	H	5 0 V	5 0 V						5 0 V	5 0 V	H	L									
		110	H	L	5 0 V	GND	GND	5 0 V		5 0 V	GND	GND	5 0 V	L	H									
		111	H	L	GND			5 0 V		5 0 V			GND	L	H									
		112	H	L	5 0 V			5 0 V		5 0 V			5 0 V	L	H									
		113	H	L	5 0 V			GND		GND			5 0 V	L	H									
		114	H	L	GND			GND		GND			GND	L	H									
		115	L	H	5 0 V			GND		GND			5 0 V	H	L									
		116	H	H	5 0 V	5 0 V	5 0 V	5 0 V		5 0 V	5 0 V	5 0 V	5.0 V	H	H									
		117	H	H	GND	5 0 V	5 0 V	5 0 V		5 0 V	5 0 V	5 0 V	GND	H	H									
																		Subgroup 9 $T_A = 25°C$		Subgroup 10 $T_A = 125°C$		Subgroup 11 $T_A = -55°C$		
t_{PHL}	3003 (Fig 11)	118	OUT		IN				GND							5 0 V	CLK_1 to Q_1	100	500	100	750	70	500	ns
		119		OUT	IN												CLK_1 to $\bar{Q}_1$							
		120											IN		OUT		CLK_2 to Q_2							
		121											IN	OUT			CLK_2 to $\bar{Q}_2$							
t_{PHL} R or S	3003 (Fig 12)	122		OUT				IN									SET_1 to $\bar{Q}_1$		550		825		550	
		123	OUT			IN											RS_1 to Q_1							
		124								IN				OUT			SET_2 to $\bar{Q}_2$							
		125										IN			OUT		RS_2 to Q_2							
t_{PLH}	3003 (Fig 11)	126	OUT		IN												CLK_1 to Q_1							
		127		OUT	IN												CLK_1 to $\bar{Q}_1$							
		128											IN		OUT		CLK_2 to Q_2							
		129											IN	OUT			CLK_2 to $\bar{Q}_2$							

TABLE II - Device: CD4013A, Electrical Test Parameters, (continued)

TABLE III. Group A inspection for device type 01 -Continued.

Symbol	MIL-STD-883 method	Cases C, D Symbol / Test No	Q_1 (1)	$\overline{Q}_1$ (2)	CLK_1 (3)	RS_1 (4)	D_1 (5)	SET_1 (6)	V_{SS} (7)	SET_2 (8)	D_2 (9)	RS_2 (10)	CLK_2 (11)	$\overline{Q}_2$ (12)	Q_2 (13)	V_{DD} (14)	Measured terminal	Subgroup 9 $T_A = 25°C$ Min	Subgroup 9 Max	Subgroup 10 $T_A = 125°C$ Min	Subgroup 10 Max	Subgroup 11 $T_A = -55°C$ Min	Subgroup 11 Max	Units
t_{PLH}	3003	130	OUT					IN	GND							5.0 V	SET_1 to Q_1	100	420	100	630	70	420	ns
R or S	(Fig 12)	131		OUT		IN											RS_1 to $\overline{Q}_1$							
		132								IN					OUT		SET_2 to Q_2							
		133										IN		OUT			RS_2 to $\overline{Q}_2$							
t_{PHL}	3004	134	OUT		IN												Q_1	30	300	40	450	25	300	
	(Fig 11)	135		OUT	IN												$\overline{Q}_1$							
		136											IN		OUT		Q_2							
		137											IN	OUT			$\overline{Q}_2$							
t_{TLH}	3004	138		OUT	IN												$\overline{Q}_1$		350		525		350	
	(Fig 11)	139	OUT		IN												Q_1							
		140											IN	OUT			$\overline{Q}_2$							
		141											IN		OUT		Q_2							
f_{CL} (max) See note O	(Fig 11)	142	OUT		IN												CLK_1		0.67		1.0		0.67	µs
		143											IN		OUT		CLK_2		0.67		1.0		0.67	µs
t_{TLHCL} (max) See note P	(Fig 11)	144	OUT		IN												CLK_1	15		15		10		µs
		145											IN		OUT		CLK_2	15		15		10		µs
tp See note Q	(Fig 11)	146	OUT		IN												CLK_1		300		450		300	ns
		147											IN		OUT		CLK_2		300		450		300	
t_{SHL}	(Fig 13)	148			IN		IN										D_1 to CLK_1		150		225		150	
t_{SHL}		149									IN		IN				D_2 to CLK_2							
t_{SLH}		150			IN		IN										D_1 to CLK_1							
t_{SLH}		151									IN		IN				D_2 to CLK_2							
t_{HHL}	(Fig 14)	152			IN		IN										D_1 to CLK_1							
t_{HHL}		153									IN		IN				D_2 to CLK_2							
t_{HLH}		154			IN		IN										D_1 to CLK_1							
t_{HLH}		155									IN		IN				D_2 to CLK_2							

NOTES

A. Pins not designated may be "high" level logic, "low" level logic or open.
B. Test numbers 17 thru 28 shall be run in sequence
C. I_{OH} = -0.25 mA at 25°C, -0.175 mA at 125°C, -0.31 mA at -55°C.
D. V_{IH1} = 3.6 V at 25°C, 3.6 V at 125°C, 3.95 V at -55°C
E. V_{IH2} = 9.5 V at 25°C, 9.35 V at 125°C, 9.75 V at -55°C.
F. I_{OL} = 0.5 mA at 25°C, 0.35 mA at 125°C, 0.65 mA at -55°C
G. V_{IL1} = 1.1 V at 25°C, 0.8 V at 125°C, 1.35 V at -55°C
H. V_{IL2} = 3.8 V at 25°C, 3.55 V at 125°C, 3.0 V at -55°C.
I. For input conditions see Figure 9
J. For input voltage conditions see Figure 10
K. The device manufacturer may, at his option, measure I_{IL} and I_{IH} at 25°C for each individual input or measure all inputs together
L. See 4.4.1(c)
M. Test numbers 101 thru 117 shall be run in sequence and the functional tests shall be performed with V_{IH} and $V_{DD} \leq 5.0$ V and ≥ 15.0 V
N. L = 0.5 V maximum and H = 4.5 V minimum
O. The maximum clock frequency (f_{CL}) requirement is considered met if proper output state changes occur with the pulse repetition period set to that given in the limits column.
P. Pulse repetition period = 100 µ sec, 50 percent duty cycle. The maximum clock transition time (t_{TLHCL}) requirement is considered met if proper output state changes occur with the rise time set to that given in the limits column.
Q. The minimum clock pulse width (t_p) requirement is considered met if proper output state changes occur with the pulse width set to that given in the limits column.

TABLE II - Device: CD4013A, Electrical Test Parameters, (continued)

TABLE III Group A inspection for device type 05

Symbol	MIL-STD-883 method	Case C, D Test No	1 Input	2 Reset	3 Q_7	4 Q_6	5 Q_5	6 Q_4	7 V_{SS}	8 NC	9 Q_3	10 NC	11 Q_2	12 Q_1	13 NC	14 V_{DD}	Meas terminal	Subgroup 1 T_A = 25°C Min	Subgroup 1 T_A = 25°C Max	Subgroup 2 T_A = 125°C Min	Subgroup 2 T_A = 125°C Max	Subgroup 3 T_A = -55°C Min	Subgroup 3 T_A = -55°C Max	Units
I_{IH}	3010	1	15.0 V	GND					GND							15 V	1		1.0		10		1.0	nAdc
I_{IH}	3010	2	GND	15.0 V													2							
I_{IL}	3009	3	GND	GND													1							
I_{IL}	3009	4	GND	GND													2							
V_{OL2}	3007	5	A	A													A		10		50		10	mVdc
V_{OH2}	3006	6	A	A													A	14.99		14.95		14.99		Vdc
V_{OH1}	3006	7	B	B	C	C	C	C			C		C	C		5.0 V	B	4.20		4.20		4.20		Vdc
V_{OL1}	3007	8	B	B	D	D	D	D			D		D	D			B		500		500		500	mVdc
V_{ICL}		9	E	E													E		3.50		3.25		3.65	Vdc
V_{IH}		10	F	F													F	1.50		1.25		1.75		Vdc
I_{SS}	3005	11	H	H												15 V	7		500		5000		500	nAdc
I_{SS}	3005	12	15 V	15 V												15 V	7		500		5000		500	nAdc
																		Subgroup 4 T_A = 25°C Min	Max					
C_I	3012	13	L						GND							GND	1		7.0					pF
C_I	3012	14		L					GND							GND	2		7.0					pF
																		Subgroup 9 T_A = 25°C Min	Max	Subgroup 10 T_A = 125°C Min	Max	Subgroup 11 T_A = -55°C Min	Max	
t_{PHL1}	3003	15	J	GND	G	G	G	G	GND		G		G	G		5.0 V	12		0.44		0.56		0.33	µs
		16															11		0.88		1.12		[illegible]	
		17															9		1.32		1.68		0.99	
		18															6		1.76		2.24		1.32	
		19															5		2.20		2.80		1.65	
		20															4		2.64		3.36		1.98	
		21															3		3.10		4.00		2.31	
t_{PLH}		22															12		0.44		0.56		0.33	
		23															11		0.88		1.12		[illegible]	
		24															9		1.32		1.68		0.99	
		25															6		1.76		2.24		1.32	
		26															5		2.20		2.80		1.65	
		27															4		2.64		3.36		1.98	
	3003	28															3		3.10		4.00		2.31	µs
t_{THL}	3004	29															J		420		550		325	ns
t_{TLH}	3004	30	J	GND													J		420		550		325	ns
t_{PHL2}	3003	31	K	K	G	G	G	G	GND		G		G	G		5.0 V	K		0.86		1.16		0.68	µs

Subgroup 7 Verify truth table, figure 3 @ $V_{DD} \leq 5.0$ Vdc and ≥ 15.0 Vdc, $V_{OL} = V_{SS} + 0.50$ Vdc, $V_{OH} = V_{DD} - 0.50$ Vdc $T_A = 25°C$.

Subgroup 8 Same test, terminal conditions and limits as subgroup 7, except T_A 125°C and -55 C

NOTES

A Each output shall be measured using the timing diagram of figure 26
B Each output shall be measured using the timing diagram of figure 27
C I_{OH} = -155 µAdc @ 25°C -105 µAdc @ 125°C, -185 µAdc @ -55°C
D I_{OL} = 250 µAdc @ 25°C 175 µAdc @ 125°C, 310 µAdc @ -55°C
E See figure 28 timing diagram
F See figure 29 timing diagram
G. Load conditions C_L 50 pF R_L 200 kΩ
H Check I_{SS} at each count state (i.e., 2^{6-1} and 2^6). (See figure 26)
J See figure 41 for test circuit and measurement points
K See figure 42 for test circuit and measurement points
For [illegible] 3

TABLE III - Device: CD4024A, Electrical Test Parameters

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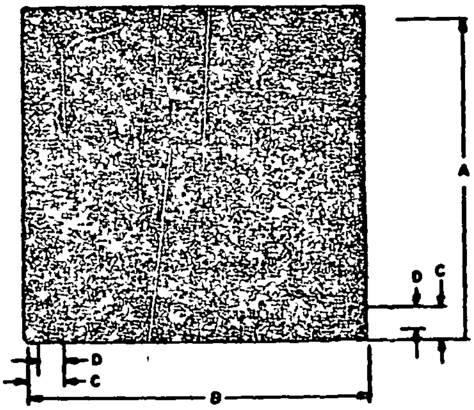
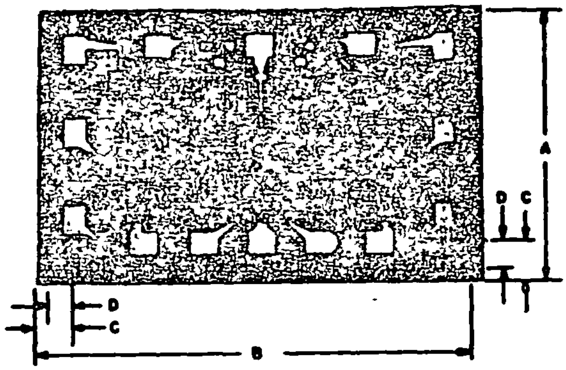
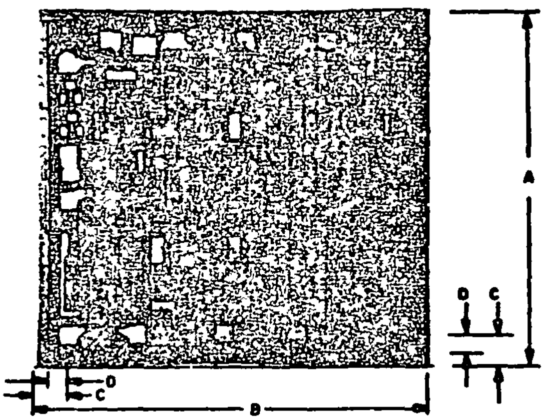


CD4011AH 92CS-22078



CD4013AH 92CS-22080

TYPE	A*		B*		C		D		CHIP THICKNESS	
	Mils	Millimeters	Mils	Millimeters	Mils	Millimeters	Mils	Millimeters	Mils	Millimeters
CD4011AH	50 – 58	1 270 – 1 473	53 – 61	1 347 – 1 549	4 – 10	0 102 – 0.254	3 3 – 4 3	0 084 – 0 109	5 – 9	0 127 – 0 228
CD4012AH	50 – 58	1 270 – 1 473	53 – 61	1 347 – 1.549						
CD4013AH	41 – 49	1 042 – 1.244	70 – 78	1 778 – 1 981						
CD4014AH	79 – 87	2 007 – 2 209	81 – 89	2 058 – 2 260	4 – 10	0 102 – 0 254	3.3 – 4 3	0 084 – 0 109	5 – 9	0 127 – 0 228



CD4024AH 92CS-22090

TYPE	A*		B*		C		D		CHIP THICKNESS	
	Mils	Millimeters	Mils	Millimeters	Mils	Millimeters	Mils	Millimeters	Mils	Millimeters
CD4023AH	53 – 61	1 347 – 1.549	53 – 61	1.347 – 1.549	4 – 10	0 102 – 0.254	3.3 – 4 3	0 084 – 0 109	5 – 9	0 127 – 0 288
CD4024AH	73 – 81	1.855 – 2 057	82 – 90	2 C83 – 2.286						
CD4025AH	49 – 57	1.245 – 1 447	51 – 59	1 297 – 1 498						
CD4026AH	89 – 97	2.261 – 2.463	89 – 97	2 261 – 2 463	4 – 10	0 102 – 0 254	3.3 – 4 3	0 084 – 0 109	5 – 9	0 127 – 0.228

** The photographs and dimensions of each COS/MOS chip represent a chip when it is part of the wafer When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip Therefore, the isolated chip is actually 7 mils (0 17 mm) larger in both the A and B dimensions*

Fig. 1 - Dimensions of microcircuit chips.

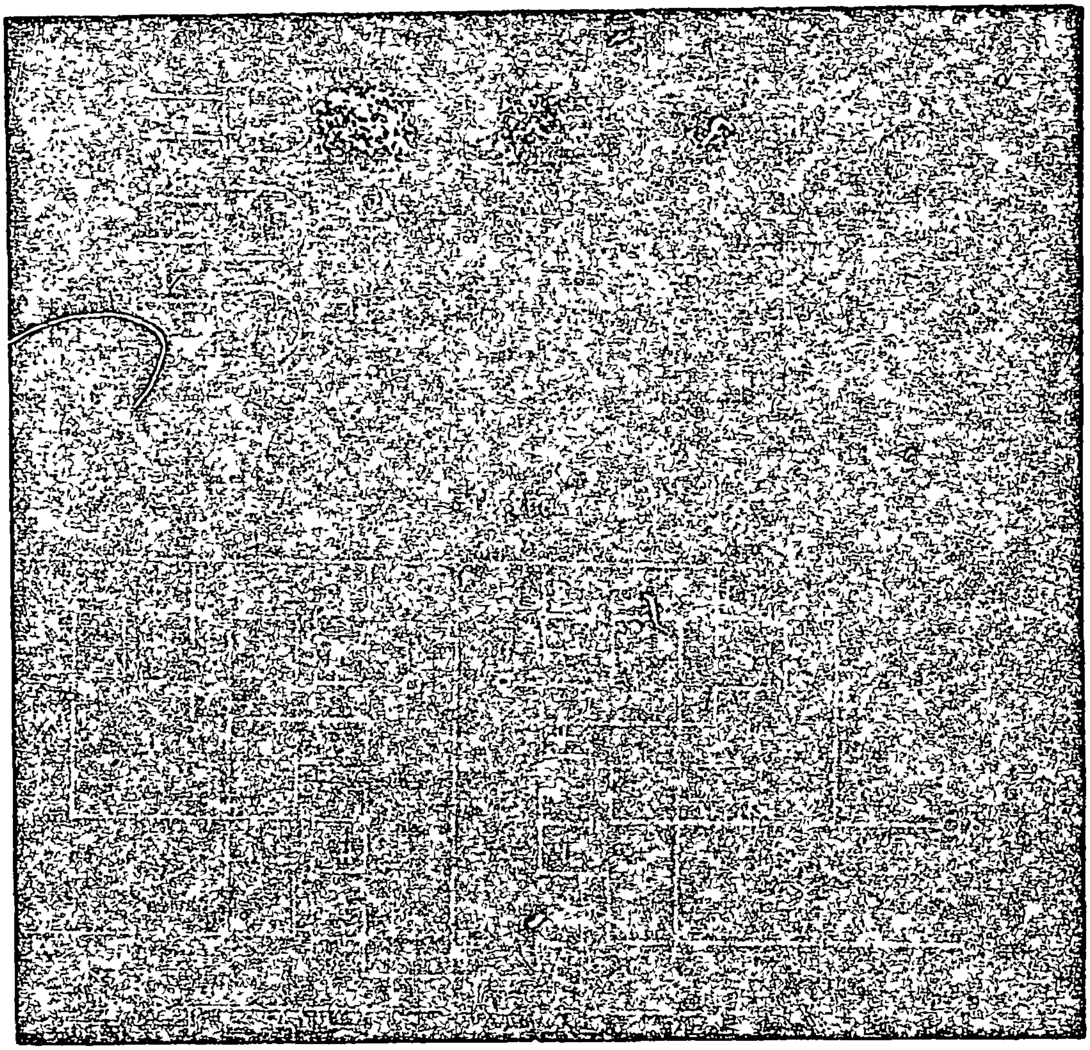


Fig. 2 - CD4011A microcircuit.

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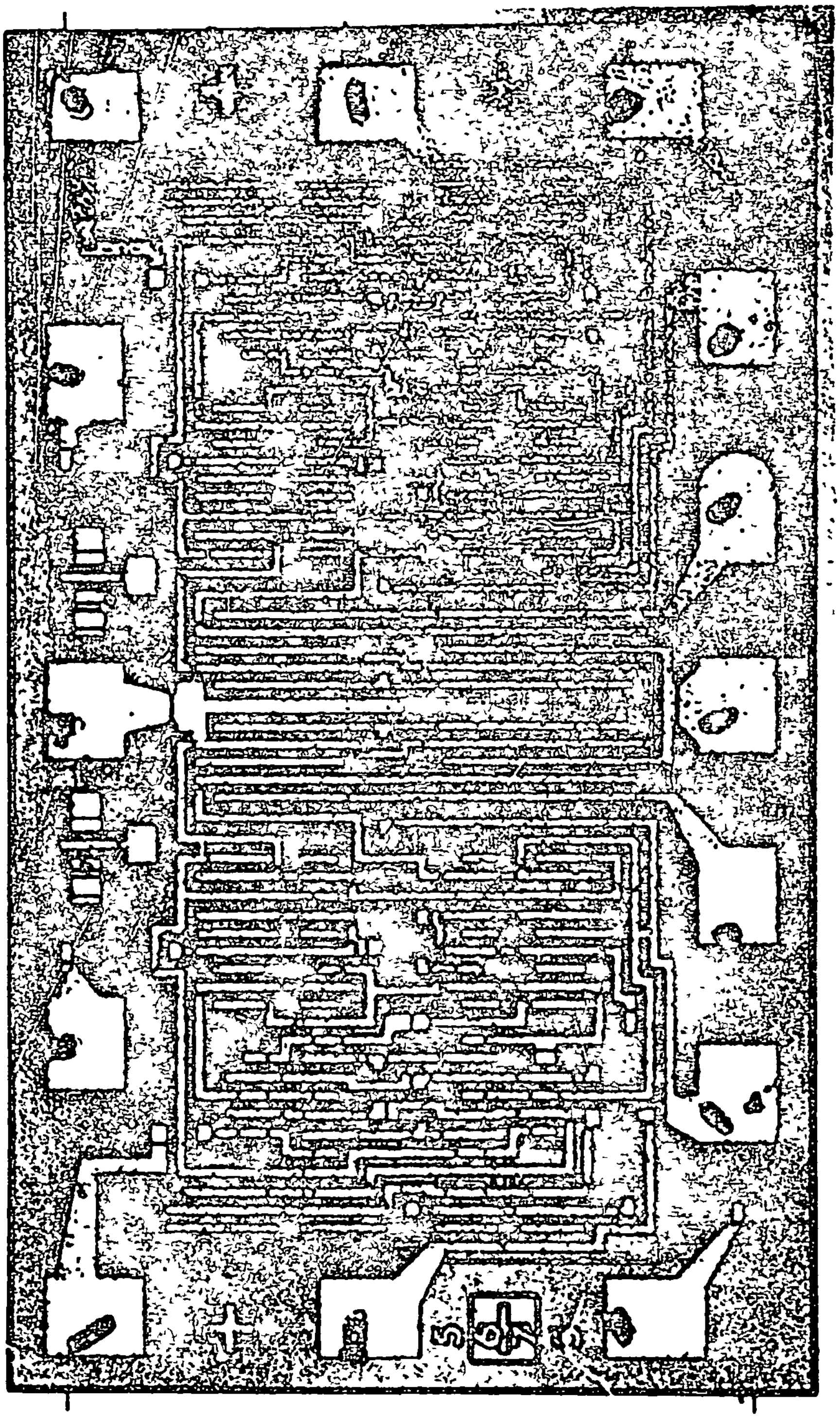

Fig. 3 - CD4013A microcircuit.

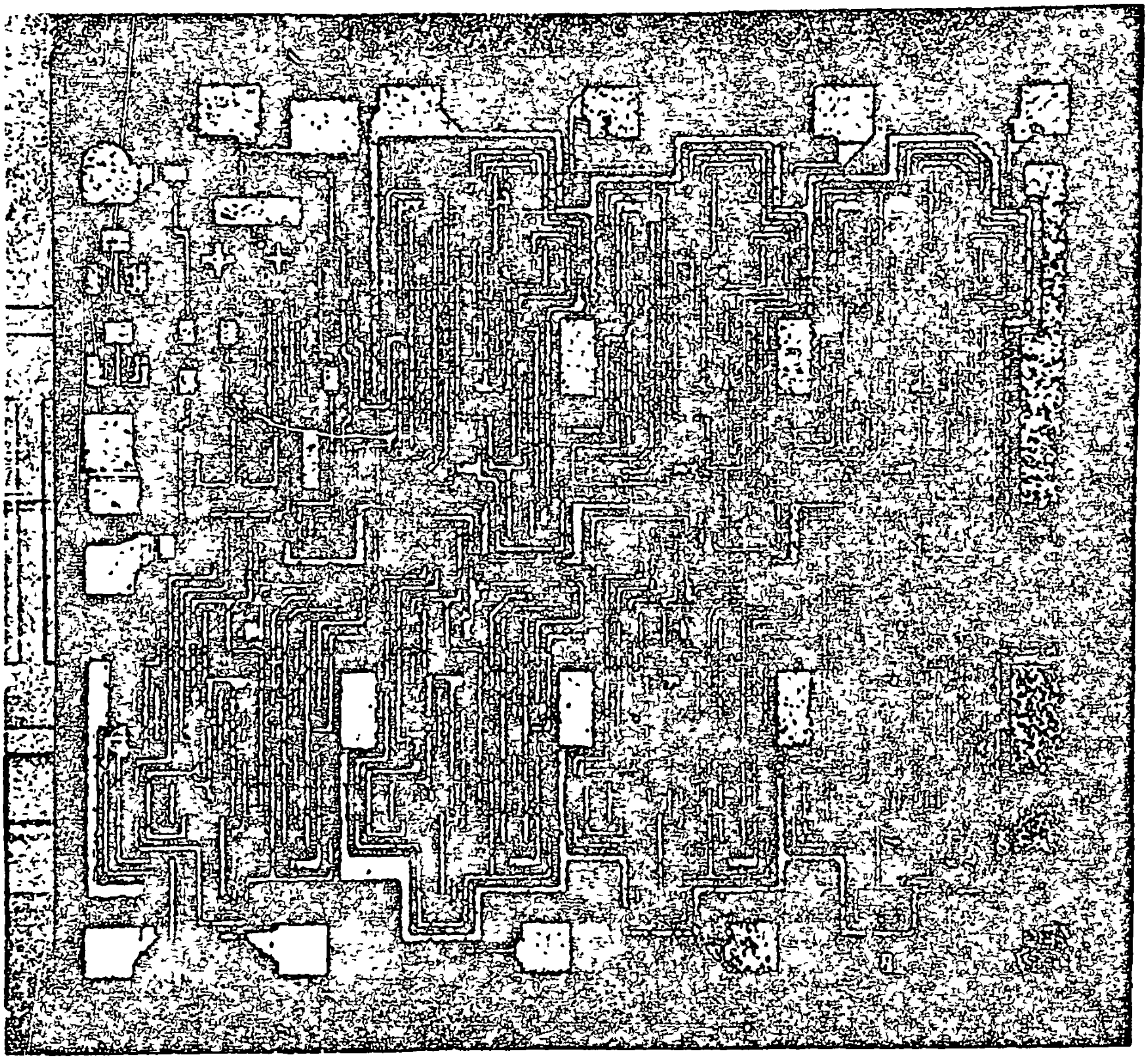

Fig. 4 - CD4024A microcircuit.

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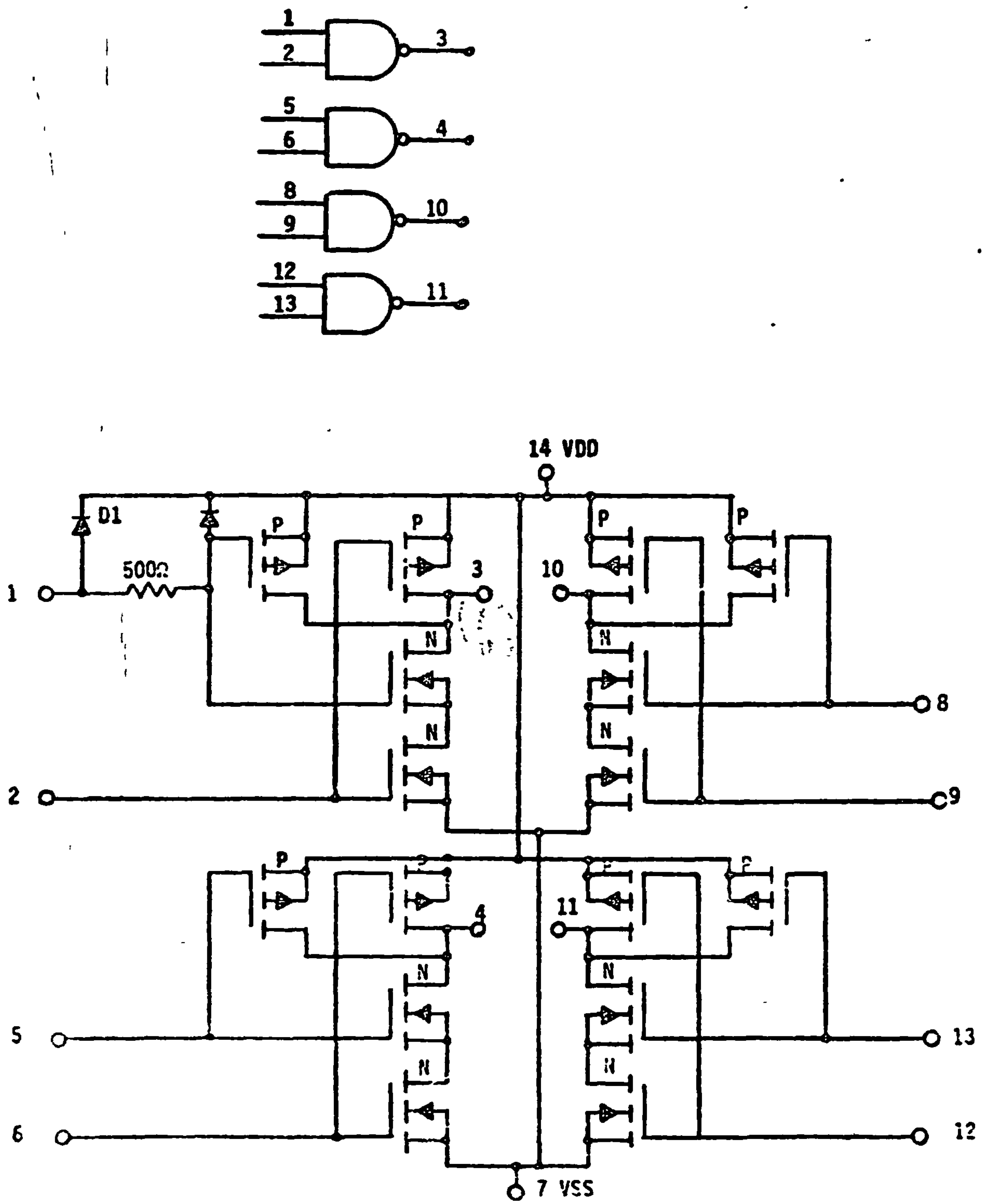


Fig. 5 - Logic and schematic diagrams for the CD4011A.

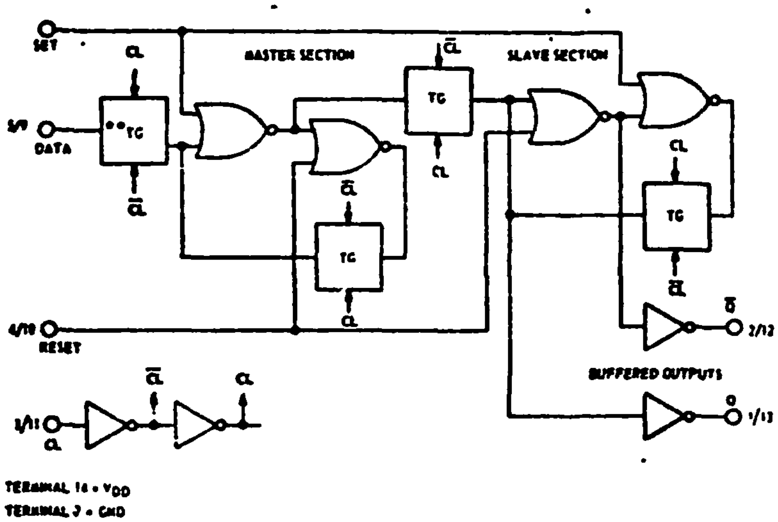


Fig. 6 - Logic diagrams for the CD4013A. (page 1 of 2 pages.)

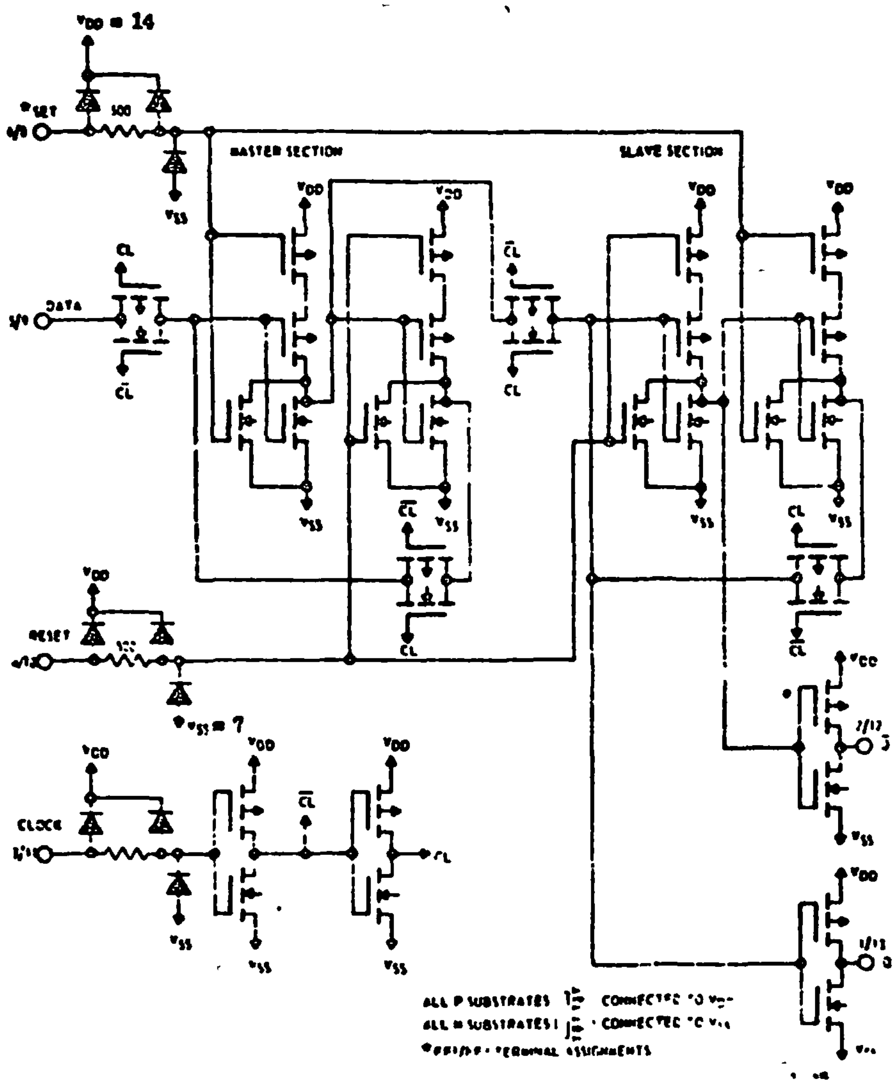
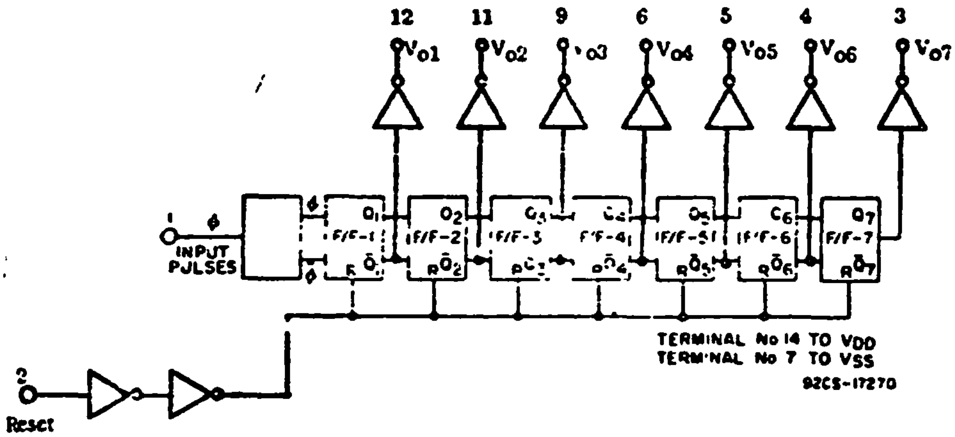


Fig. 6 - Schematic diagrams for the CD40134. (Page 2 of 2 pages.)



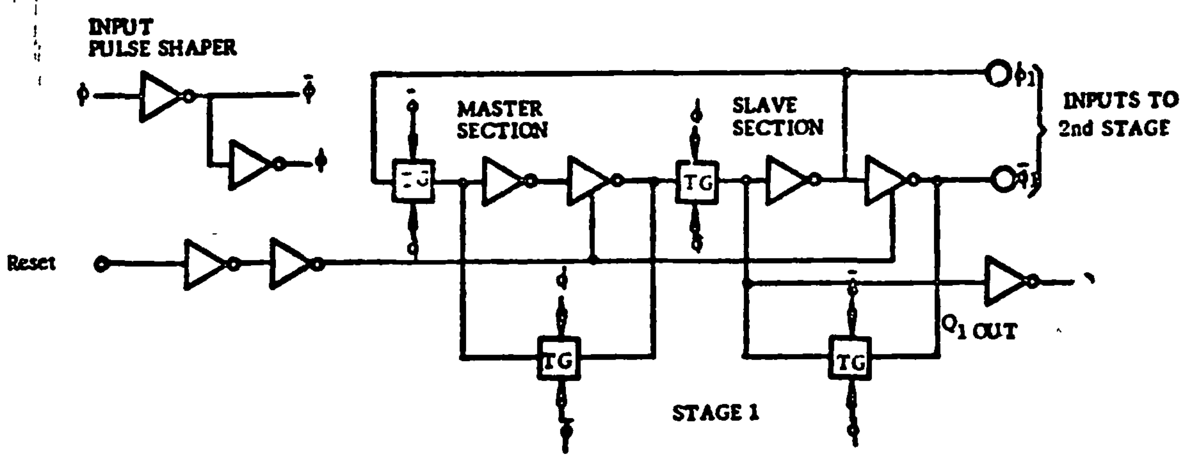


Fig. 7 - Functional and logic diagrams for the CD4024A. (Page 1 of 2 pages.)
Input Pulse Shaper and one of seven binary stages are shown.

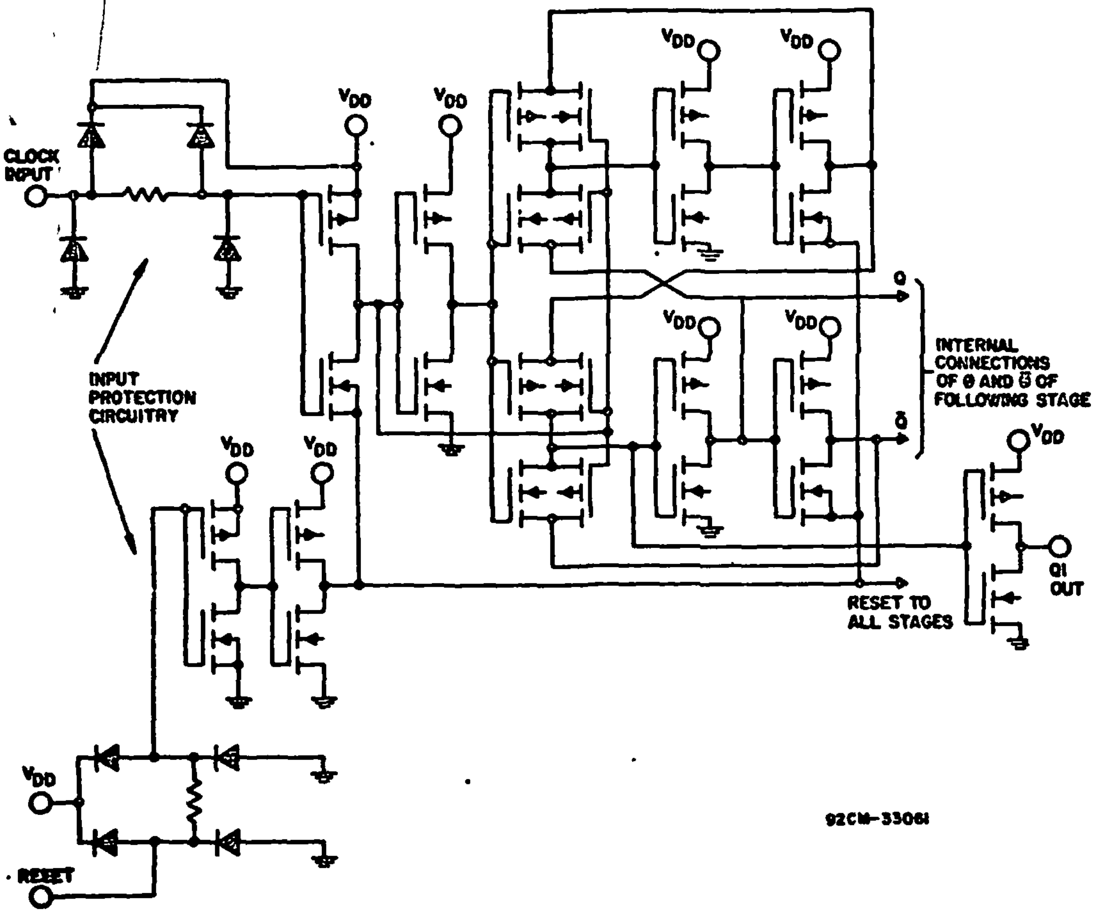


Fig. 7 - Schematic diagram for the CD4024A. (Page 2 of 2 pages.)

Table IV - Microcircuit Complexity Factors

Type	Si Area	No. of Active Elements	Number of Inputs	Number of Outputs
CD4011A	1.9 mm^2	13	8	4
CD4013A	2.1 mm^2	64	8	4
CD4024A	4.2 mm^2	134	2	7

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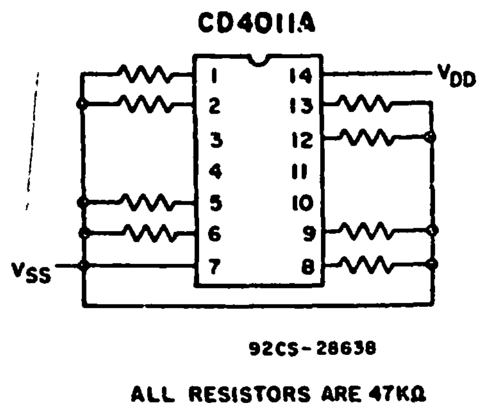
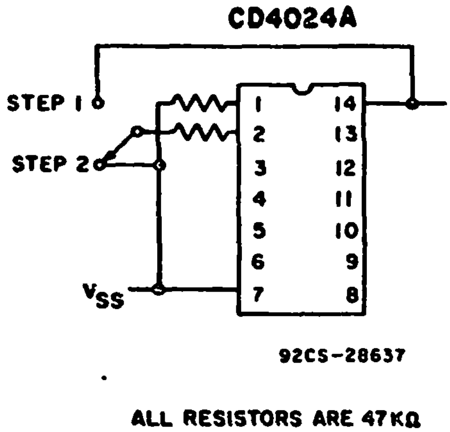
SECTION IV

TEST VOLTAGE AND BIAS

The choice of bias was dictated by the desire to further accelerate the life testing process by stressing the n-channel transistor to possibly the worst-case condition. The available evidence suggests that the n-channel transistor in CMOS microcircuits is the weak link when biased to the off condition (gate is low with respect to drain). The drain-to-source and drain-to-gate potentials set up under this bias accelerate movement of the positively charged (usually sodium) particles. These particles are thought to accumulate in the oxide, thereby neutralizing the effect of the negatively biased gate and setting up a mechanism for potential leakage. The biases used are shown in the pin connection diagrams of Fig. 8. The operating voltage was chosen as 12.5 volts dc to conform to the MIL-M-38510 detail specifications.





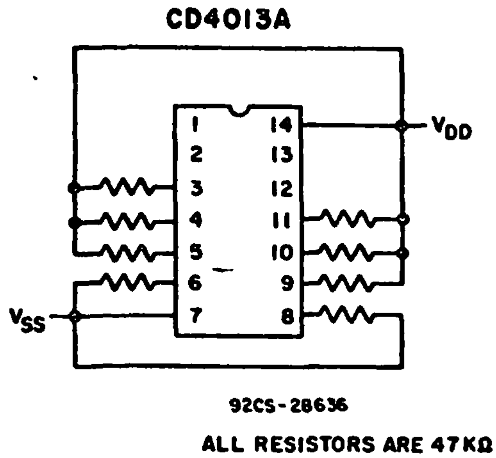


Fig. 8 - Bias connection diagrams.

SECTION V

THE TEST

The test matrix was developed and is shown in Fig. 9. Devices were selected from three lots in each type to represent broad process variations. The program encompasses three life-test temperatures. Each lot is represented by twenty test devices in each life test for a total of sixty test devices of each type. Each test sample of twenty test devices included, in addition, five control devices which were monitored at each measurement point together with the test devices, but were not life-tested.

Prior to the beginning of the contract, trial runs were started. Data from those runs prompted the introduction of more measurement points for the 250°C as well as the 200°C life test. The testing at each measurement point was broadened to include 125°C, and -55°C measurements.

As the final results of the 250°C test became available and the first results of the 200°C tests started to come in, a desirability to evaluate the impact of the manufacturing environment upon the test results was recognized. In order to accomplish this, the high temperature burn-in ovens were transferred from Findlay, Ohio plant to Somerville, N.J. upon the completion of the 200°C test. There were devices left over from some of the lots made for this program. These devices were used to run repeat tests. Two device types: CD4011A and CD4013A were tested at 250°C and 200°C. The task was accomplished by the engineering personnel, and the measurements at down periods were done utilizing Somerville's facilities. These tests were completed at no additional cost to the government.

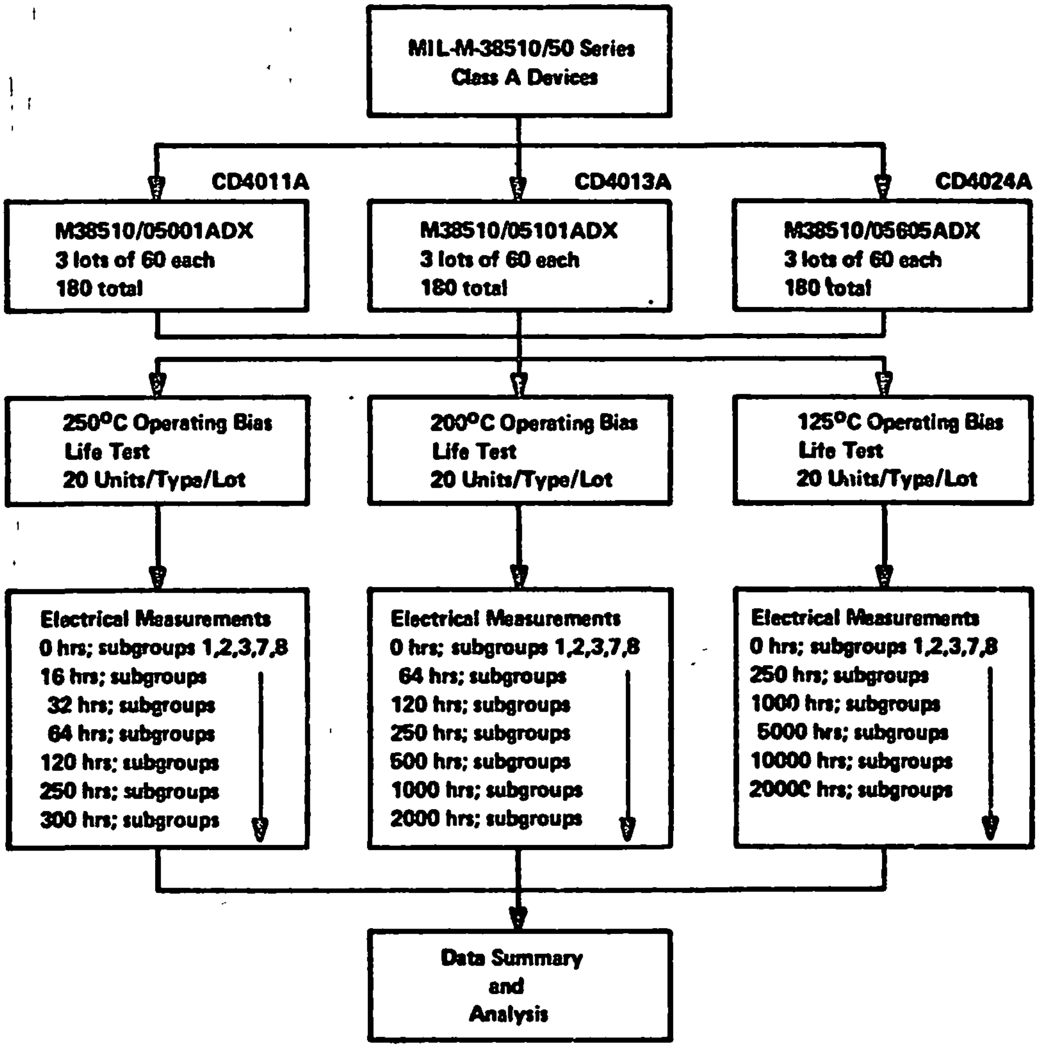


Fig. 9 - Test Matrix.

SECTION VI
DISCUSSION OF TEST RESULTS

Summary of Failure Attributes

The summaries of the failure attributes and cumulative percentage of failures are presented in Tables V-XVII. The results of the 250°C and the 200°C repeat tests are shown in Tables XI-XIV. The sample size does not always remain twenty devices because those devices that were lost due to malfunctioning of the automated test equipment and those which were continuity rejects because of poor socket connections were removed from the count. The data from these tables were then plotted on log normal graph paper to present the cumulative percent of failures versus the test time. Each graph contains the resultant curves from the basic tests at the three test temperatures for each of the three device types, Figs. 10 through 12. The repeat test plots superposed over the basic test plots are shown for the CD4011A and the CD4013A at the 200°C and 250°C test temperatures to demonstrate the degree of repeatability of results for the tests conducted under different environments, Figs. 13 and 14. The curves for the CD4013A and the CD4024A at 250°C test temperatures, Figs. 11 and 12, are continued with dashed lines at the points where the tests have been terminated on one of the three test lots having accumulated at least 50 percent cumulative failures.

The cumulative-failures distributions, as they appear in the graphs of Figs. 10 through 14, strongly suggest that at each test temperature the visible distributions represent portions of the familiar "S" shaped curve which is characteristic of the three regions in the life span of a microcircuit*.

* "Evaluation of Microcircuit Accelerated Test Techniques," Final Technical Report RADC-TR-76-218 for Rome Air Development Center, Griffiss AFB, N.Y., 13441

TABLE V - Summary of Cumulative Failures for Device Type CD4011A

250°C Test

Lot No. \ Hours	16	32	64	120
5361740	0/19	0/19	0/17	16/17
6153050	1/20	6/20	8/20	16/20
6153060	2/20	2/19	7/19	18/19
3-Lot Total	4/59	8/59	15/56	50/56
3-Lot % Failure	7	14	27	89

TABLE VI - Summary of Cumulative Failures for Device Type CD4013A

250°C Test

Lot No. \ Hours	16	32	64
6153080	5/20	7/20	15/15
6123240	2/20	2/20	
5393020	1/20	4/20	
3-Lot Total	8/59	13/60	15/15
3-Lot % Failure	14	36	100

TABLE VII - Summary of Cumulative Failures for Device Type CD4024A

250°C Test

Lot No. \ Hours	16	32	64
6201050	2/20	13/19	
6202230	7/19	10/18	18/18
6201060	3/20	15/20	
3-Lot Total	12/59	38/57	18/18
3-Lot of Failure	20	66	100

TABLE VIII - Summary of Cumulative Failures for Device Type CD4011A

200°C Test

Lot No. \ Hours	64	120	250	500	750	1500	2000
5361740	0/20	0/20	0/20	0/20	0/20	6/16	11/18
6153050	1/19	1/19	1/19	1/19	1/19	4/19	14/17
6153060	1/19	1/18	1/18	1/18	1/18	6/18	6/18
3-Lot Total	2/58	2/57	2/57	2/57	2/57	16/55	31/53
3-Lot % Failure	3.4	3.5	3.5	3.5	3.5	29	58

TABLE IX - Summary of Cumulative Failures for Device Type CD4013A

200°C Test

Lot No. \ Hours	64	120	250	500	1000
6153080	0/19	1/17	1/16	3/16	16/16
6123240	0/20	0/18	0/18	0/19	17/19
2-Lot Total	0/39	1/35	1/35	3/35	33/35
2-Lot % Failure	0	2.8	2.8	8.5	94

TABLE X - Summary of Cumulative Failures for Device Type CD4024A

200°C Test

Lot No. \ Hours	64	120	250	500
6201050	0/20	2/20	11/19	17/19
6202230	0/20	1/20	7/20	17/19
6201060	0/20	0/20	7/20	20/20
3-Lot Total	0/60	3/60	25/59	54/58
3-Lot % Failure	0	5	42	93

TABLE XI - Summary of Cumulative Failures for Device Type CD4011A

250°C Repeat Test

Lot No. \ Hours		16	32	64	96	128	160
5361740 6153050 6153060	3-Lot Total	1/38	1/38	3/38	3/38	15/38	31/38
3-Lot % Failure		2.6	2.6	7.9	7.9	39.5	82

TABLE XII - Summary of Cumulative Failures for Device Type CD4013A

250°C Repeat Test

Lot No. \ Hours		8	16	32	48	64
6153080 6123240	2-Lot Total	2/38	3/38	5/38	8/38	24/38
2-Lot % Failure		5.3	7.9	13	21	63

TABLE XIII - Summary of Cumulative Failures for Device Type CD4011A

200°C Repeat Test

Lot No. \ Hours		64	128	250	500	1000	1500	2000	2500
5361740 6153050 6153060	3-Lot Total	0/38	3/38	4/38	4/38	6/38	7/38	11/38	30/38
3-Lot	% Failure	0	8	11	11	16	18	29	79

TABLE XIV - Summary of Cumulative Failures for Device Type CD4013A

200°C Repeat Test

Lot No. \ Hours	64	128	250	500	1000	1500	2000
6123240	2/38	2/38	2/38	3/38	9/38	19/38	37/38
% Failure	5	5	5	8	23	50	97

TABLE XV - Summary of Cumulative. Failures for Device Type CD4011A

125°C Test

Lot No. \ Hours	168	500	1000	2500	5000	10,000	15,000	20,000
5361740	0/19	0/19	0/18	0/18	0/18	0/18	0/18	0/18
6153050	0/20	0/20	0/18	0/18	0/18	0/17	0/15	0/15
6153060	0/20	0/20	0/20	0/20	1/18	1/18	1/18	1/18
3-Lot Total	0/59	0/59	0/56	0/56	1/54	1/53	1/51	1/51
3-Lot % Failure	0	0	0	0	1.8	1.9	2.0	2.0

TABLE XVI - Summary of Cumulative Failures for Device Type CD4013A

125°C Test

Lot No. \ Hours	168	500	1000	2500	5000	10,000	15,000	20,000
6153080	0/20	0/20	0/20	0/20	0/20	0/20	-	0/20
6123240	0/20	0/20	0/20	0/20	0/20	0/20	-	0/20
5393020	0/20	0/20	0/20	1/20	4/20	4/20	-	4/20
3-Lot Total	0/60	0/60	0/60	1/60	4/60	4/60	-	4/60
3-Lot % Failure	0	0	0	1.7	6.7	6.7	-	6.7

TABLE XVII - Summary of Cumulative Failures for Device Type CD4024A

125°C Test

Lot No. \ Hours	168	500	1000	2500	5000	10,000	15,000	20,000
6202230	0/20	0/20	0/20	2/20	-	2/20	2/20	3/20
6201050	0/20	0/20	2/20	3/20	-	4/20	4/20	4/20
6201060	0/20	0/20	0/20	0/20	-	1/20	2/20	2/20
3-Lot Total	0/60	0/60	2/60	5/60	-	7/60	8/60	9/60
3-Lot % Failure			3.3	8.3		11.7	13.3	15

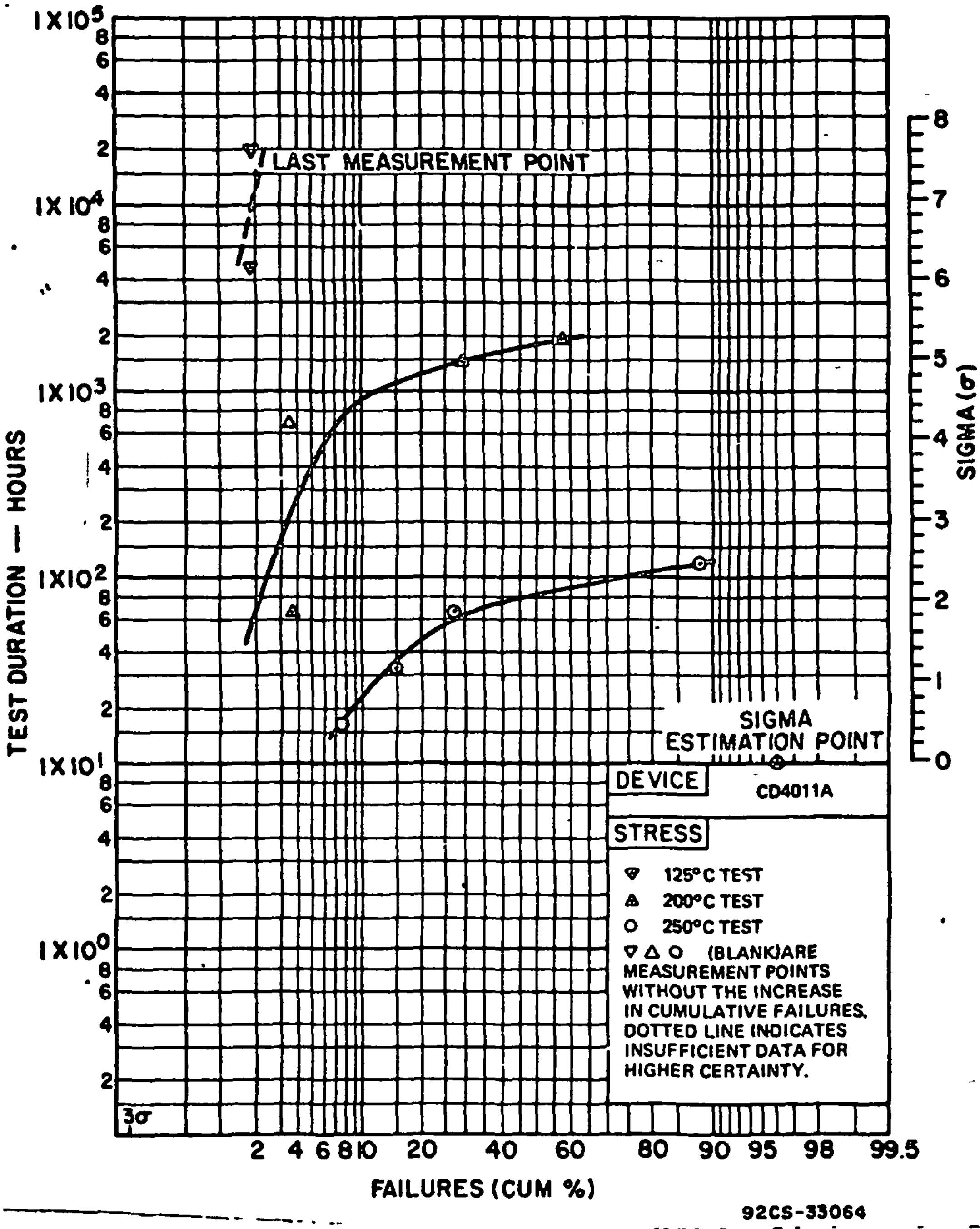


Fig. 10 - Distribution of test failures for CD4011A.

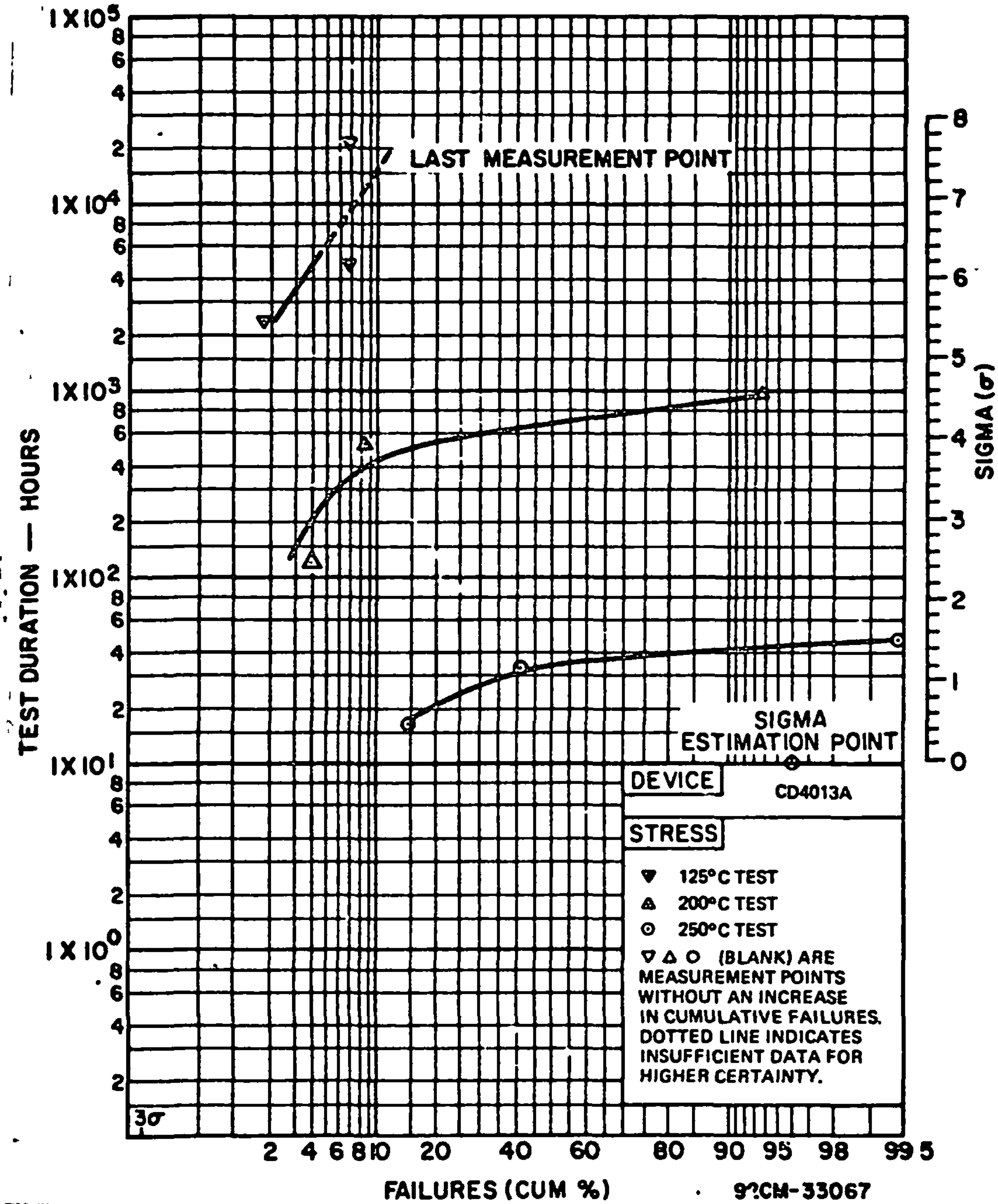


Fig. 11 - Distribution of test failures for CD4013A.

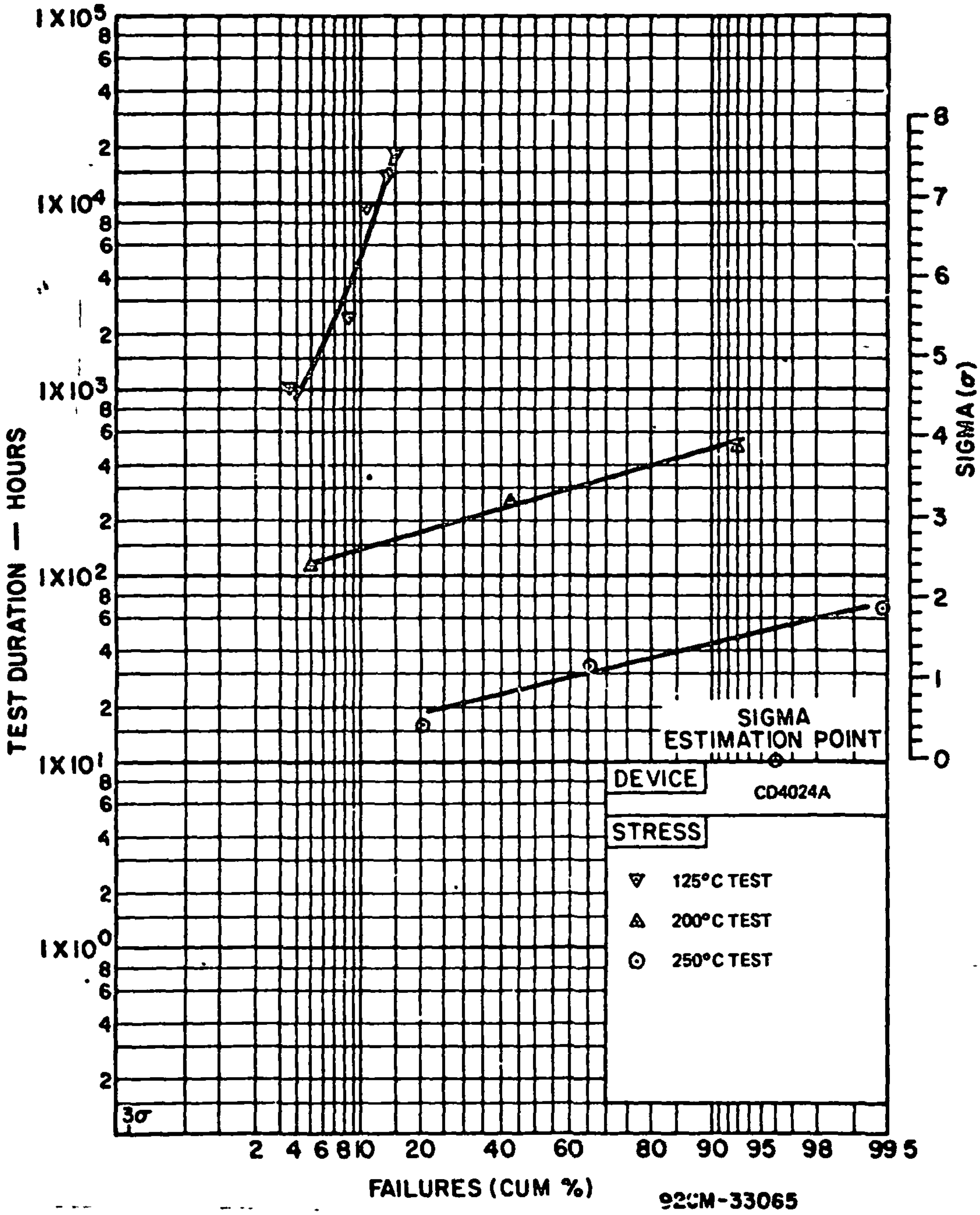


Fig. 12 - Distribution of test failures for CD4024A.

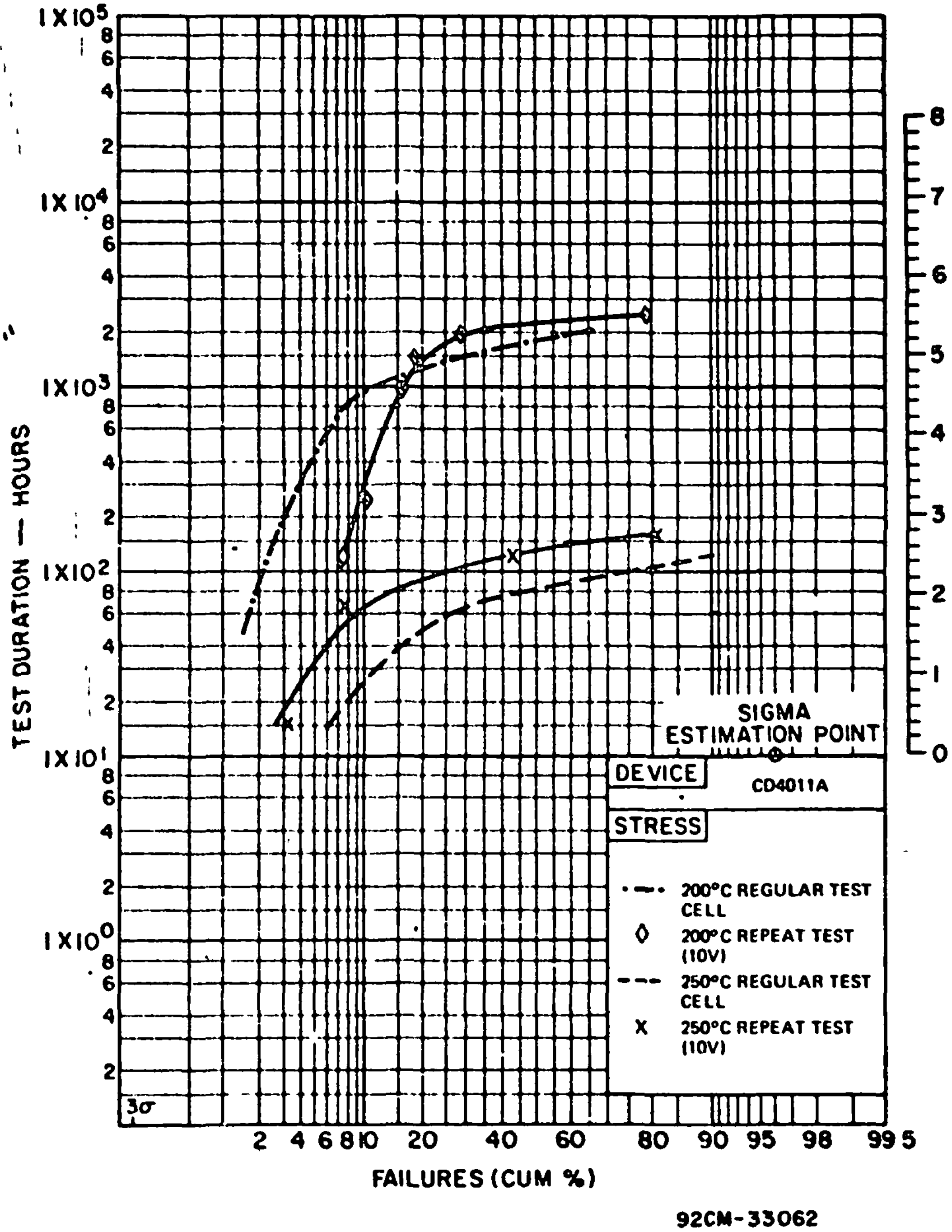


Fig. 13 - Distribution of test failures for CD4011A - Repeat test.

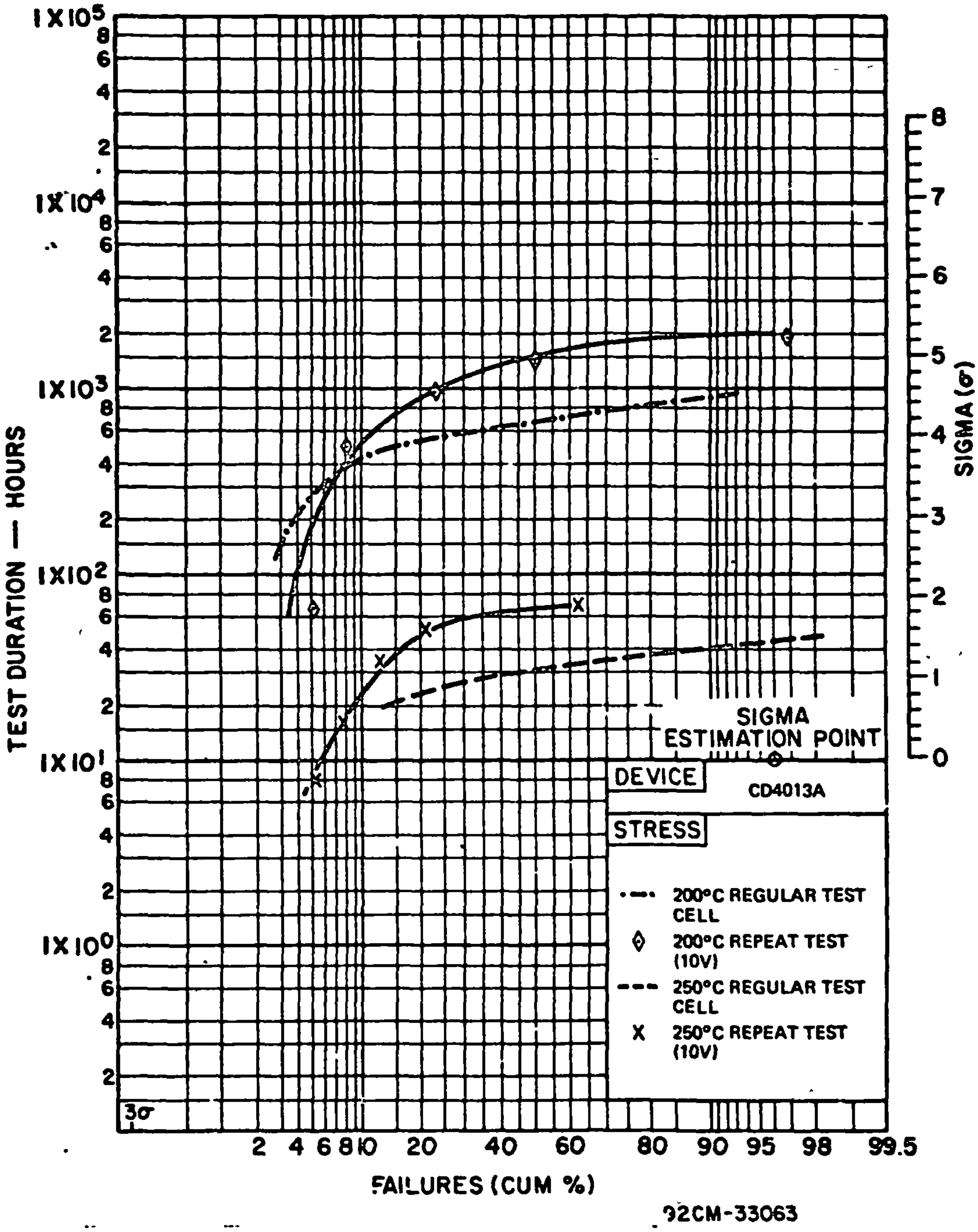


Fig. 14 - Distribution of test failures for CD4013A - Repeat test.

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The lower tail regions which represent the early failures (infant mortality) distributions are largely taken out by the standard 125°C burn-ins to which all test devices had been subjected prior to the accelerated life tests. The useful life regions are the regions with constant or decreasing failure rates. These regions are clearly evidenced at 200°C and 125°C test temperatures. The third region shown in the S curve is the wear-out region; this region is represented by the main distribution. The presence of this region is apparent in the 250°C and the 200°C test temperature curves. The characteristic feature of this wear-out region is increasing failure rate. The wear-out region has not been reached by the tests conducted at 125°C.

The 250°C test curves, with a possible exception of the CD4011A, exhibit a compression of the useful life region to such an extent that it becomes indistinguishable from the wear-out region for all practical purposes. Moreover, the available data suggest that the onset of wear-out could have occurred quite early in the test, and that it might have been caused by the exceeding of a yet unknown threshold peculiar to that temperature. Because of these factors it is impossible to estimate the effect of the 125°C burn-ins on the results of accelerated testing at 250°C.

The transition from the useful life region to the wear-out region is most clearly defined by the 200°C test curves for the CD4011A and the CD4013A. The onset of the wear-out region is identified by the knee in the curve where the failure rate begins to increase. The location of this knee is at about 1000 hours for the CD4011A, about 400 hours for the CD4013A, and could be estimated to be at about 100 hours for the CD4024A. The repeat tests (Figs. 13 and 14) conducted at two test temperatures, i.e., 250°C and 200°C, with the CD4011A and the CD4013A, have confirmed a) the existence of fairly well defined regions in the life of the tested microcircuits, i.e., the useful life region and the wear-out region, and b) the location of the knee in the "S" curve, the transition from one region into the other, which is characterized by the changing failure rate from constant to increasing.

It should be noted that the main distribution at both 250°C repeat tests occurs noticeably later than those of the first test. The reason for this was found to be the life-test voltage: 10 volts during the repeat test instead of 12.5 volts due to an inadvertant error in setting up the test in a different location and by different personnel. This error does not, however, diminish the validity of the confirmation of the existence of the main distributions with increasing failure rate.

At the test temperature of 125°C, none of the three tested device types has reached the wear-out region at the last down time of 20,000 hours. It should be noted that two of the three tested lots of the CD4011A as well as two of the three CD4013A lots have had zero cumulative failures at the 20,000-hour down time. With the available data, the existence of the wear-out regions at 125°C can only be surmised.

The importance of identifying the three regions in the life span of a microcircuit lies in the following. The wear-out region is useful in determining the activation energy between various test temperatures, which in turn provides a tool for projecting life at application temperature based on the results of accelerated life-test. The location of this region allows one to locate the "knee", the point of the changing failure rate and the end of the useful life of the device. It is suggested that it is important to locate the "knee" in time as well as to determine the percent cumulative failure at this point. The determination of the MTTF, for example, should be done using test results obtained from distributions with sigma common to the use temperature and the accelerated test temperature. The knowledge of the early failure region is helpful in assessing the effectiveness of burn-in schedules.

Activation Energy

The activation energy between 200°C and 250°C was estimated on the basis of main distributions (wear-out region); it was found to vary from

type to type: 1.35 eV for CD4011A, 1.25 eV for CD4013A, and 1.0 eV for CD4024A. A more accurate determination of the activation energy and/or verification of the observed type-to-type variations would require a third data point. The wear-out region for the test temperature of 125°C was not reached at 20,000 hours, consequently the third data point was not obtained. The method of graphical estimation of activation energies for each device type is shown in Fig. 15. The times at which 50-percent cumulative failure is reached during tests made on each device type at 200 and 250°C are plotted on the graph of Fig. 15 as a function of temperature, and the resulting points joined by a straight line. Another line with the same slope and passing through the estimation point will intersect the activation energy scale at the value of the activation energy for that device type.

The Effect of Temperature and The Burn-Ins

Prior to the accelerated life tests, all devices were burned-in at 125°C with the standard burn-in schedule for class-A CMOS microcircuits: two 24-hour bias burn-ins and one 240-hour dynamic burn-in. It is evident from the 200°C and the 125°C test curves that there were more failures during the early stages of these tests than would be compatible with the constant failure-rate line through the knee, thus indicating decreasing failure rates. These early failures must come from the tail end of the "infant mortality" or "freak" distributions extending into the useful life region. The implications of this finding are that a) the 125°C, 1000-hour life tests presently in use are likely to detect failures which are part of the "infant mortality" distribution when used for lot acceptance, b) the CMOS microcircuits may be inherently more reliable than the results of the 125°C, 1000-hour life tests tend to indicate, and c) better reliability may be realized through improving the burn-ins so that more of the remaining "infant mortality" distribution is removed from the population. It seems impractical, however, to simply extend the duration of the 125°C burn-ins currently in use. Further acceleration of burn-ins by using higher temperature and/or voltage would be suggested for consideration in the development of such burn-ins.

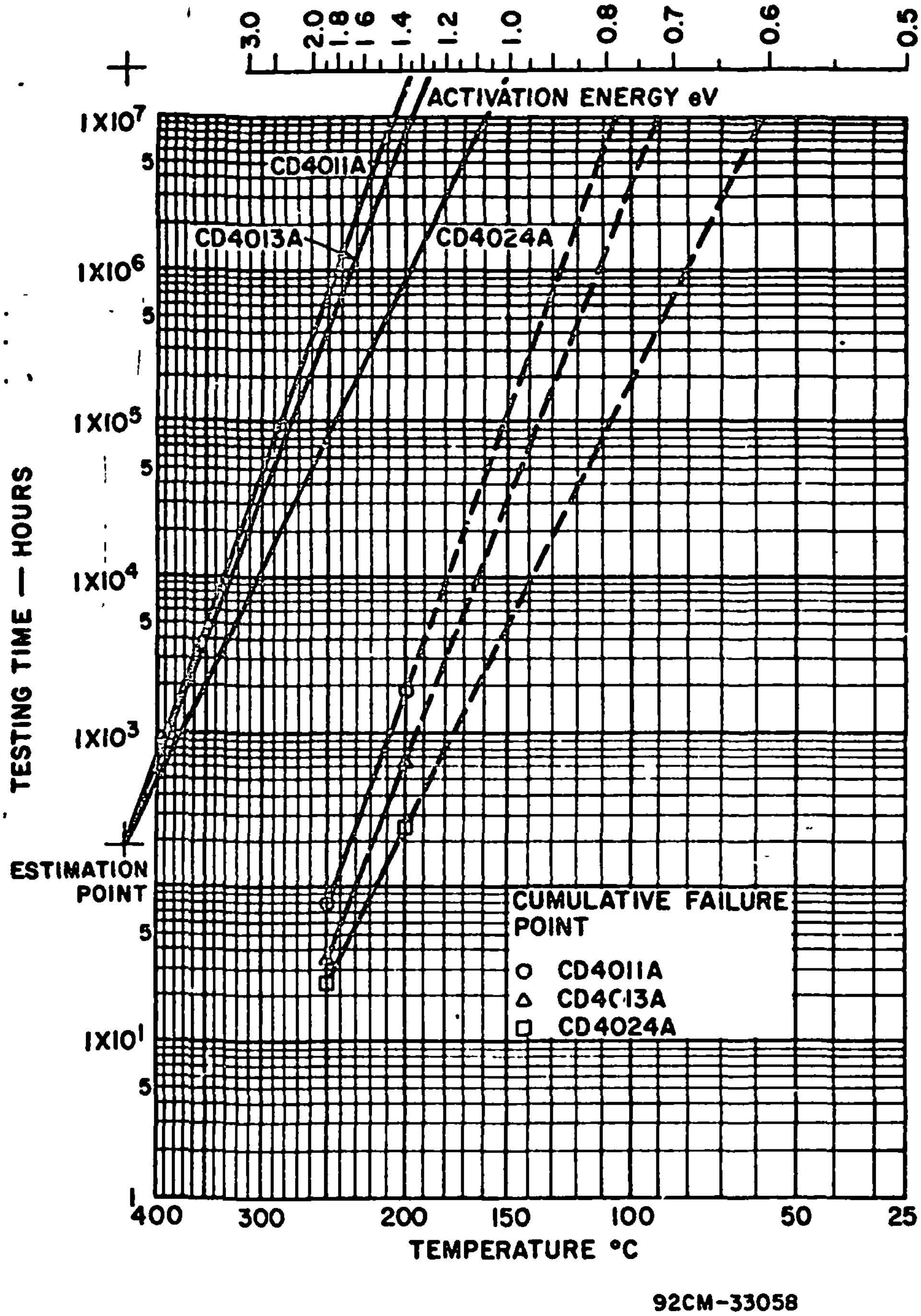

Fig. 15 - Estimation of activation energy.

Device Complexity

The test results indicate that the "longevity" of a device depends upon the complexity of a device when criticized to MIL-M-38510 electrical end points. The longevity is defined here as the 50-percent failure point, and is located in the wear-out distribution. Of all the factors listed in Table IV, the number of active devices on a chip most closely correlates to the longevity of a microcircuit. Table XVIII summarizes this observation for the 250°C test cell and for the 200°C cell, two temperatures for which 50 percent failure points were reached. This illustration presents a sufficient case against making generalizations when devising acceptance criteria for life test, that is, generalizations based on one technology and applied to another or based on test results of one device type and applied to all device types within the same technology.

Cost Considerations

In the production environment, efficiency and trouble-free operations are extremely important. This study uncovered two problem areas which were the consequence of the high-temperature material used for sockets on the life-test panels and for the device carriers. The material, aromatic copolyester, is extremely brittle. Constant breakage of the life-test sockets necessitated costly repairs and resulted in delays that upset test schedules. Breakage of the very fragile clips that hold devices in carriers resulted in delays in testing as well as in the automated measurements. It was also found that the carriers warp under exposure to 250°C. A warped carrier creates pin-contact problems in test sockets of the automated measuring equipment, and good devices can be rejected as continuity failures. These rejects must be ver[illegible] other means of testing, with a resultant loss of time. All these factors [illegible]buted significantly to the cost of running the accelerated test. An asses[illegible] the relative cost of running accelerated life tests was made and is prese[illegible] in Table XIX. All costs are normalized to 125°C for easy comparison.

TABLE - XVIII - Time to 50% Cumulative Failure Point Versus Complexity of Device

Test Temperature	CD4011A 13 Active Elements	CD4013A 64 Active Elements	CD4024A 134 Active Elements
250°C	80 hrs.	33 hrs	25 hrs
200°C	1800 hrs	650 hrs	250 hrs

TABLE XIX

RELATIVE COSTS

High Temperature Facilities

Factors	Temperature 125°C	200°C	250°C
Oven Cost	1	1	1.25
Socket Cost	1	2	7.5
Socket Life	1	1	2.5
Oven Life	1	2	2
Maintenance	1	1.25	1.5
Total	1	5	70

SECTION VII

FAILURE ANALYSIS

CD4011A - The most prevalent type of failure is the loaded output voltage, followed closely by the input leakage. These two most common types of failure, depending upon the severity (amount of deviation from the norm), may result in an eventual functional failure.

CD4013A - The most prevalent types of failure are the total leakage (Iss) and the input leakage. Again, depending upon the severity of the leakage, it may eventually result in a functional failure. The ten Iss tests specified by the MIL-M-38510 detail specification representing different states of the flip-flop do not appear as failures with the same frequency. States which have clock input "high" exhibit more frequent Iss failures than do other states. The "D" input tends to have more frequent input leakage failures than other inputs.

CD4024A - The most prevalent type of failure is the total leakage (Iss). All nine Iss tests except one show equal frequency of occurrence. The ninth test (input and reset are high) exhibits considerable lower frequency of occurrence.

Tables XX, XXI, and XXII give for the 250°C test cell the means, the standard deviation, and the high value at each measurement point on the per lot basis for the surviving devices at two measurement temperatures, 25°C and 125°C. Figs. 16, 17, and 18 represent plots of mean averaged over three lots for each type and at two temperatures. The surviving units are defined as those for which the readings did not reach the clamped values. Clamped values are the upper limits of the instrument range to which the automated measurement system is set.

TABLE XX – I_{SS} Trend with Time for the M38510/05001ADX (CD4011A)

Time			0 Hrs			16 Hrs.			32 Hrs.			64 Hrs.			120 Hrs.		
	Lot #	Test #	50	51	52	50	51	52	50	51	52	50	51	52	50	51	52
		Unit	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA
25°C Measurements	5361740	Mean	0 17	0 16	0 44	0 75	1 1	2 7	0 83	1 07	1 39	1	1 04	1 27	0 63	10 8	0 37
		S D	0 27	0 36	0 59	0 25	0 76	0 19	0 18	0 13	0 17	0 20	0 09	0 33	0 3	30 8	0 32
		H V	0 7	1	1 3	1 1	1 1	3	1 2	1 2	1 6	1 4	1 3	1 5	159 8	108 4	1 2
	6153050	Mean	0 65	1 01	1 37	2	1 32	3 4	3 73	3 22	5 55	3 55	3 48	5 21	2 2	1 76	0 70
		S D	0 4	0 1	0 16	2 2	0 44	0 56	6 31	1 28	7 87	2 3	0 91	3 8	2 89	1 19	0 14
		H V	1 2	1 2	1 7	3 1	3 1	5 6	30 4	8 2	38	11 8	6 3	19 7	10 8	3	0 9
	6153060	Mean	0 07	0 88	1 13	0 9	1 4	3 4	0 67	1 2	1 55	1 61	1 93	2 23			
		S D	0 09	0 1	0 12	1 2	1 1	2 3	0 35	0 32	0 34	0 78	0 54	0 75			
		H V	0 2	1	1 4	5 7	5 5	12 5	1 2	2	2 5	3 5	3 1	4 7			
125°C Measurements		Unit	μA	μA	μA	μA	μA	μA	μA	μA	μA	μA	μA	μA	uA	μA	μA
	5361740	Mean	100 2	67	74	125 7	100 3	72 1	131.7	96 9	73 4	134 6	89 8	72 8	301 4	457 5	115
		S D	19 6	39 7	16	26 4	19	14 6	28 4	20	15	33 4	23 5	15 6	361 1	415.1	24 4
		H V	136	109	98	172	132	97	188	137	103	193	133	104	1393	751	158
	6153050	Mean	143 7	64 1	126 2	175 1	103 8	130	180 1	97 1	125 2	196 1	89 1	230 8	259	395 2	103 6
		S D	53 3	36 6	31	47 7	26 2	36 5	53	17 6	39 7	60 4	22 8	295 2	137 1	509 2	30 8
		H V	222	103	197	265	124	197	284	125	200	292	117	1086	499	227	176
	6153060	Mean	63	79 6	51 3	76 7	79.3	48 5	77 1	78 6	49	45	42 8	27 7			
		S D	26	26 4	18 5	28	25.1	19 8	30 1	25 7	19 22	21	18 2	15 3			
		H V.	138	140	91	134	136	84	132	136	83	86	80	55			

S.D. - Standard deviation

H.V. - High value

Low values were zero

TABLE XXI – I_{SS} Trend with Time for the M38510/05101ADX (CD4013A)

Time			0 Hrs.			16 Hrs			32 Hrs.			64 Hrs.			120 Hrs.
	Lot #	Test #	50	55	60	50	55	60	50	55	60	50	55	60	
		Unit	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	
25°C Measurements	5393020	Mean	0 0	0 0	0 0	1 1	0 8	1 4	0 0	0 0	0 5				
		S D	0 0	0 0	0 0	4 6	0 8	1 0	0 0	0 0	1 0				
		H V	0 0	0 0	0 0	20 0	3 0	3 0	0 0	0 0	3 0				
	6123240	Mean	0 0	0 0	0 0	0 0	0 5	1 2	0 0	0 0	0 1				
		S D	0 0	0 0	0 0	0 0	0 8	1 1	0 0	0 0	0 2				
		H V	0 0	0 0	0 0	0 0	3 0	3 0	0 0	0 0	1 0				
	6153080	Mean	0 0	0 0	0 0	0 8	1 6	2 0	41 0	87 0	95 0	31 0	3 1-8	3 9 8	
		S D	0 0	0 0	0 0	2 4	2 6	2 6	140 0	360	390 0	89 0	1 1-7	1 3 7	
		H V.	0 0	0 0	0 0	7 0	11 0	11 0	570 0	1500	1600	330	4 4-7	5 0-7	
125°C Measurements		Unit	μA	μA	μA	μA	μA	μA	μA	μA	μA	μA	μA	μA	
	5393020	Mean	0 093	0 07	0 092	0 27	0 12	0 19	0 67	2 5	2 4				
		S D	0 013	0 015	0 013	0 65	0 01	0 013	2 5	3 5	2 8				
		H V	0 12	0.12	0 12	3 0	0 13	0 14	11 0	13 0	8 2				
	6123240	Mean	0 11	0 12	0 12	0 28	0 19	0 21	0 08	11 0	0 13				
		S D	0 01	0 009	0 01	0 75	0 36	0 46	0 02	0 08	0 1				
		H V	0 13	0 13	0 13	3 5	1 7	2 2	0 13	0 42	0 52				
	6153080	Mean	0 072	0 074	0 074	0 24	0 57	0 64	0 84	0 5	0 53	0 58	0 28	0 35	
		S D	0 009	0 007	0 008	0 54	1 2	1 4	2 4	1 1	1 2	0 61	0 41	0 5	
		H V	0 09	0 09	0 09	2 3	4 5	5 4	9 1	3 5	3 8	1 6	1 1	1 3	

S.D. – Standard deviation

H.V. – High value

Low values were zero

TABLE XXII – I_{SS} Trend with Time for the M38510/05605ADX (CD4024A)

Time			0 Hrs			16 Hrs.			32 Hrs.			64 Hrs.			120 Hrs.
	Lot #	Test #	60	63	67	60	63	67	60	63	67	60	63	67	
		Unit	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	nA	
25°C Measurements	6201050	Mean	45 81	53 35	55 8	33 4	35 7	34 2	41 7	103 7	82 3				
		S D	109 36	110 98	110 57	129	125 2	123	96 6	246 3	177.5				
		H V	418	417	418	565	564	555	578	580	565				
	6201060	Mean	1 11	3 35	2 88	0	9 6	8 75	11	12	12				
		S D	1 11	2 39	2 86	0	0 7	1 9	24	24	23				
		H V	4	11	13	0	11	16	114	113	112				
	6202230	Mean	2 31	4	2 25	1 42	10 85	8 4	20	20	17 2	782	779	761	
		S D	5	5 63	1 1	5 95	6	0 95	29	27 8	26 1	287	285	293	
		H V	23	27	4	26	37	9	99	103	101	1160	1153	1142	
125°C Measurements		Unit	μA	μA	μA	μA	μA	μA	μA	μA	μA	μA	μA	μA	
	6201050	Mean	0 42	0 54	0 54	0.70	0 77	0 73	1 2	1 2	1 9				
		S D	0 61	0 83	0 83	1 86	1 89	1 84	1 7	1 7	1 4				
		H V	2 34	2 96	2 95	8.4	8 41	8 41	6 03	5 76	5 24				
	6201060	Mean	0 18	0 21	0 21	0 17	0 19	0 18	3	3	3				
		S D	0 06	0 10	0 10	0 06	0 11	0 12	5	4	4				
		H V	0.37	0 55	0.56	0 29	0 28	0 28	0 5	0 49	0 50				
	6202230	Mean	0 12	0 12	0 12	0 24	0 22	0 22	0 45	0 44	0 43	7 58	All clamped		
		S D	0 02	0 02	0 02	0 29	0 27	0 27	0 50	0 48	0 47	2 75			
		H V	0 2	0 21	0 21	1.4	1 35	1 32	1 7	1 7	1 6	9 39			

S.D. - Standard deviation

H.V. - High value

Low values were zero

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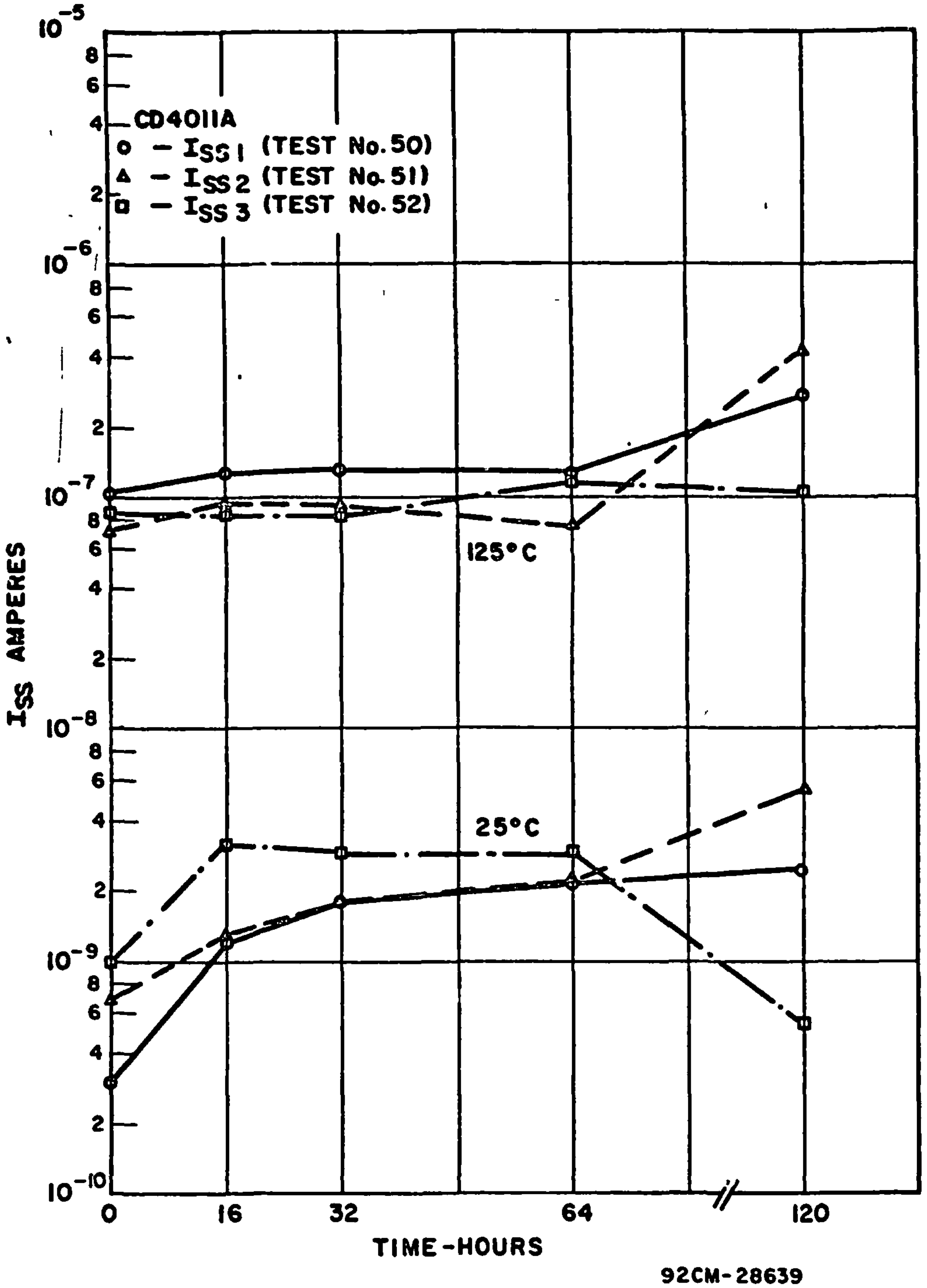


Fig. 16 - CD4011A; I_{SS} vs time; three-lot average of mean.

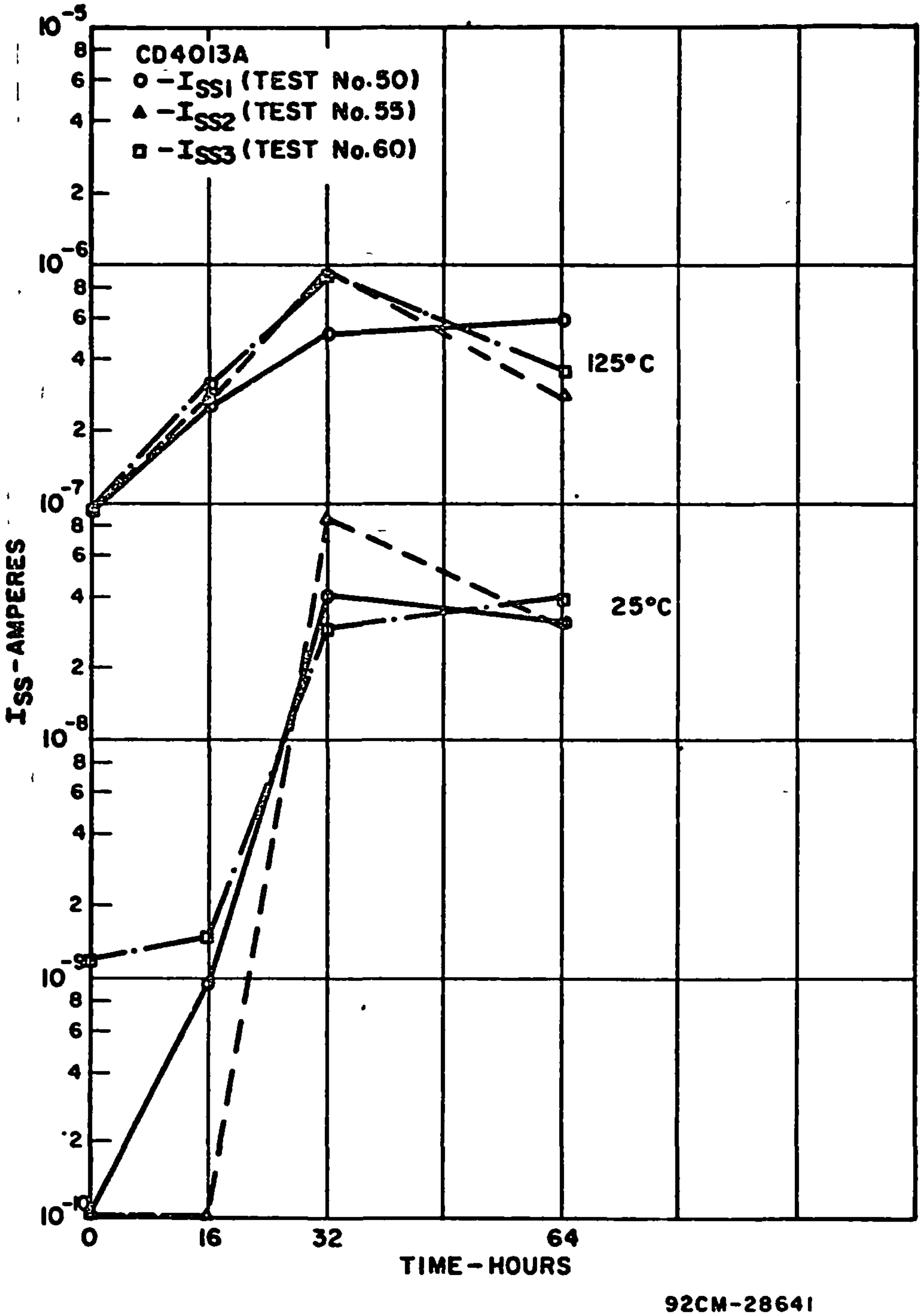


Fig. 17 - CD4013A; I_{SS} vs time; three-lot average of mean. Only one lot was kept on life test to 64 hours. Value of I_{SS} < 0.1 nA are plotted on the base line.

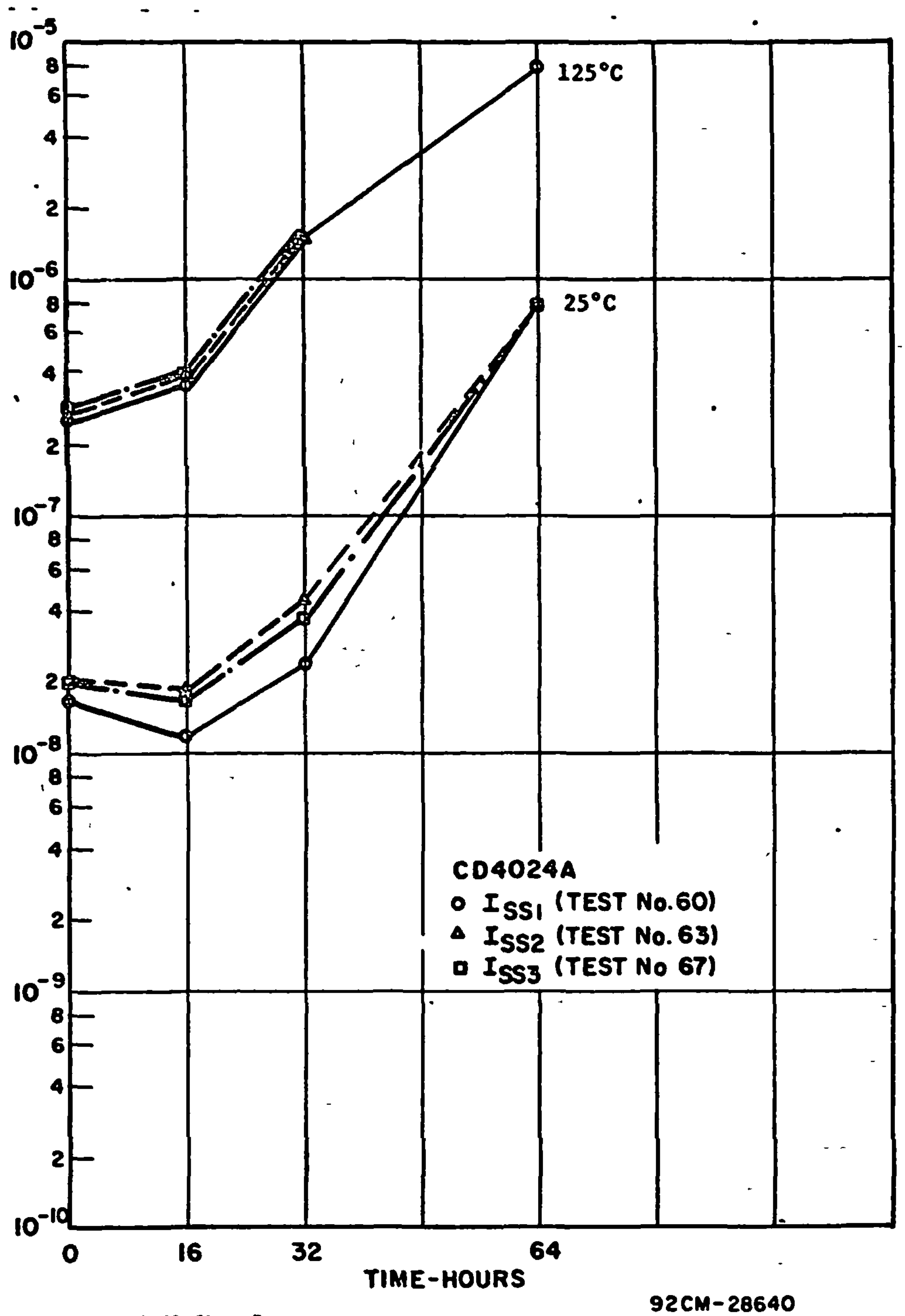
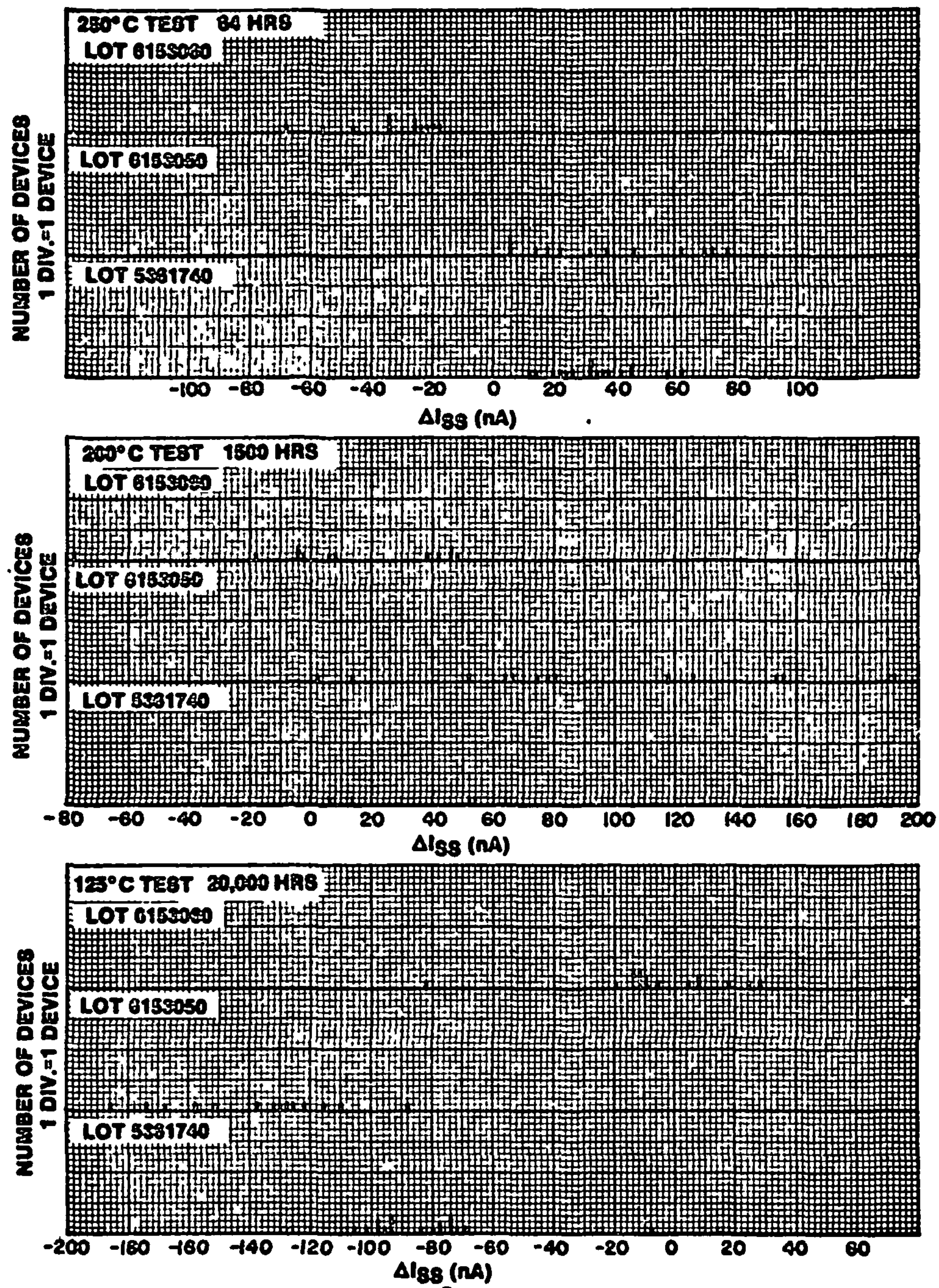
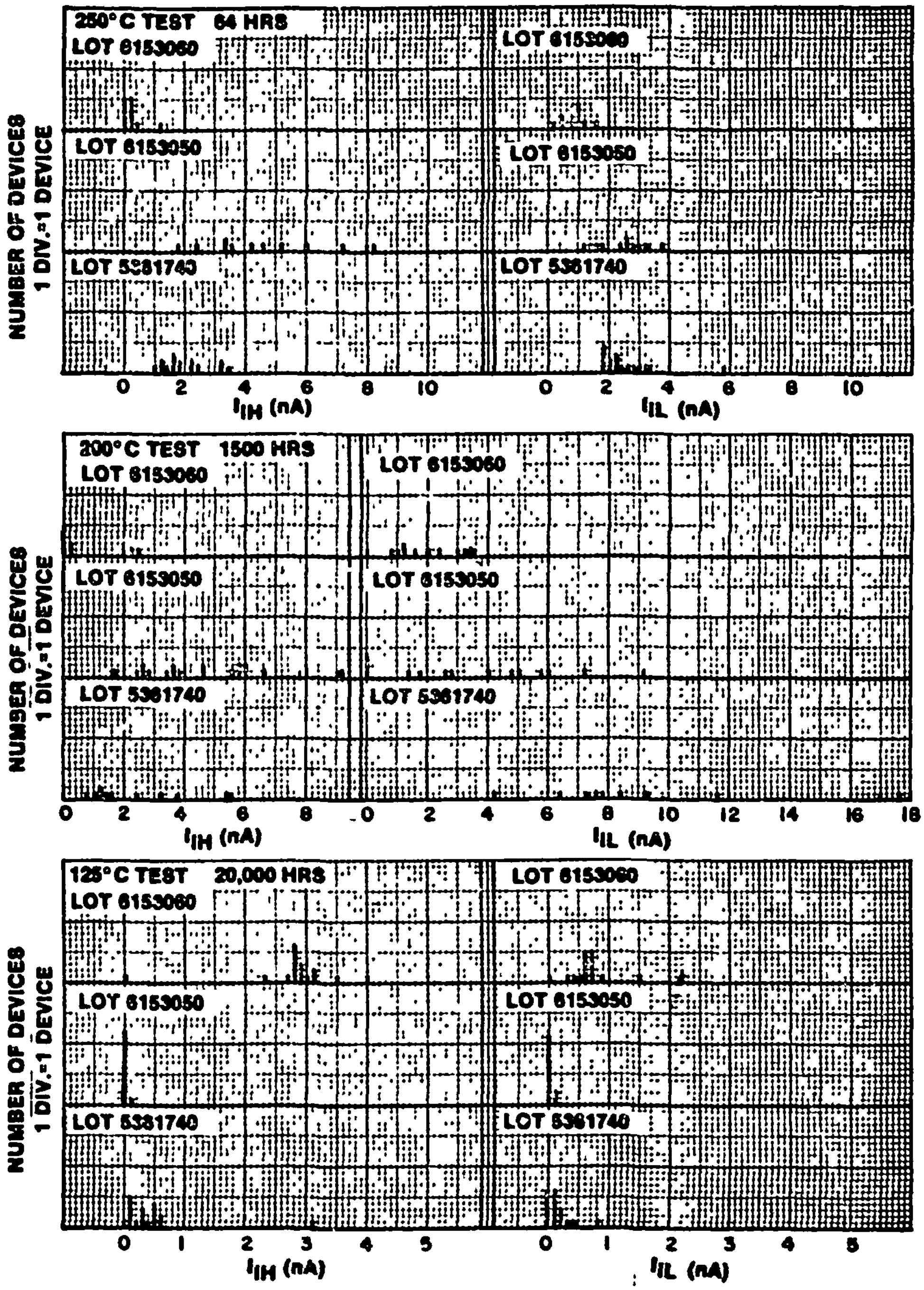


Fig. 18 - CD4024A; I_{SS} vs time; three-lot average of mean. Only one lot was kept on life test to 64 hours.



Distribution of ΔI_{SS} at V_{DD}=15V, T=125°C, for device type CD4011A.



Distribution of I_{IH} and I_{IL} at V_{DD}=15V, T=125°C, for device type CD4011A.

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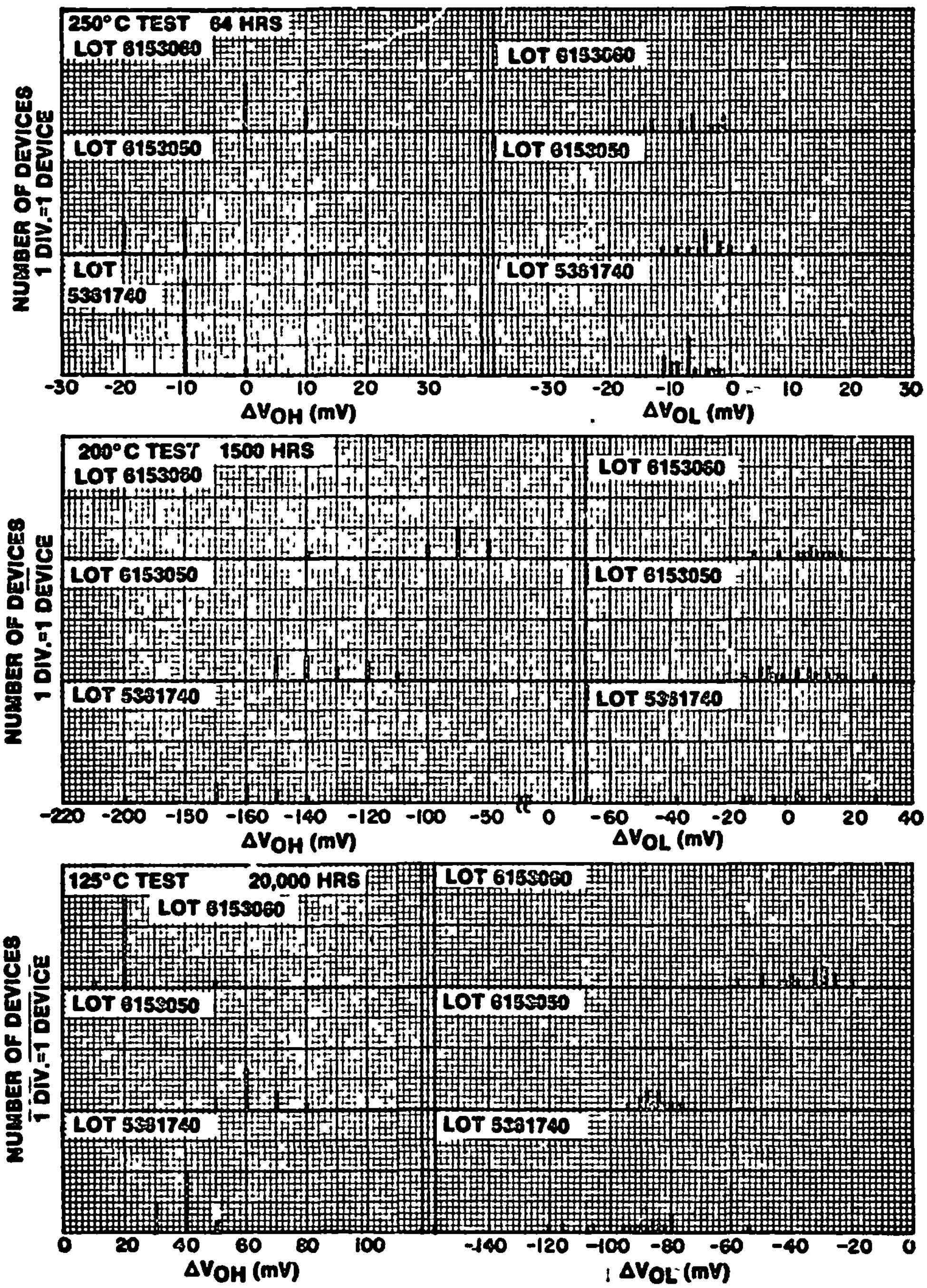
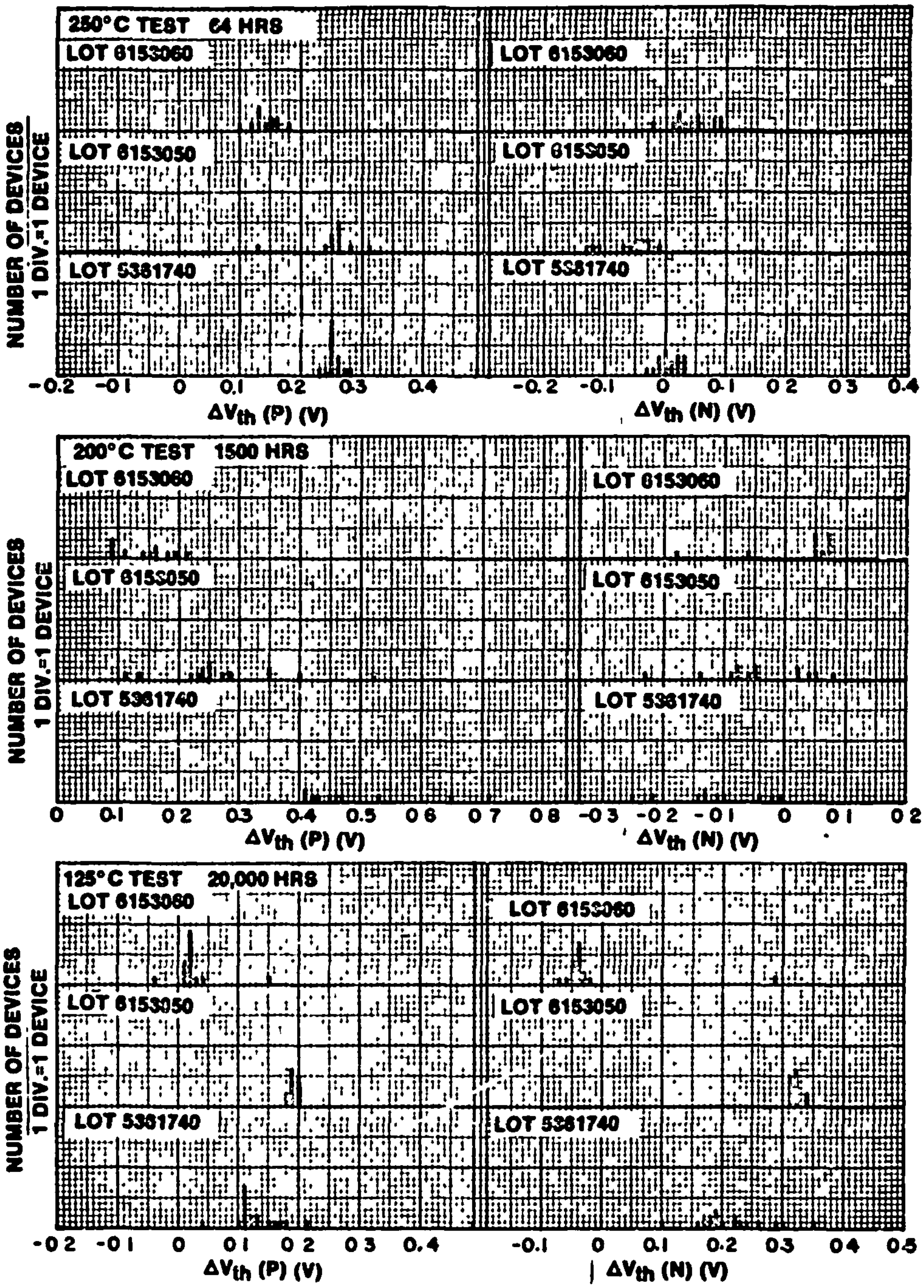
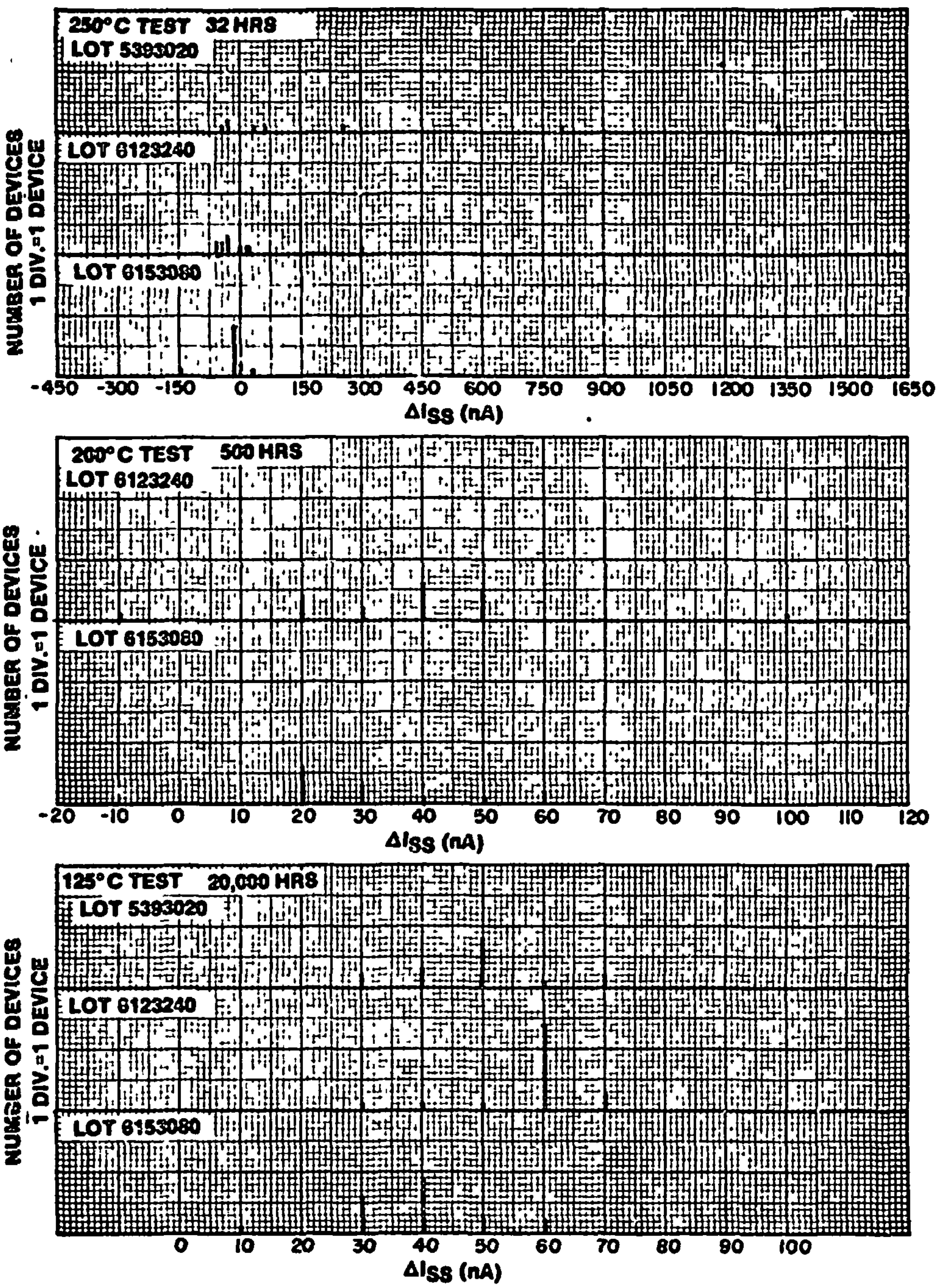


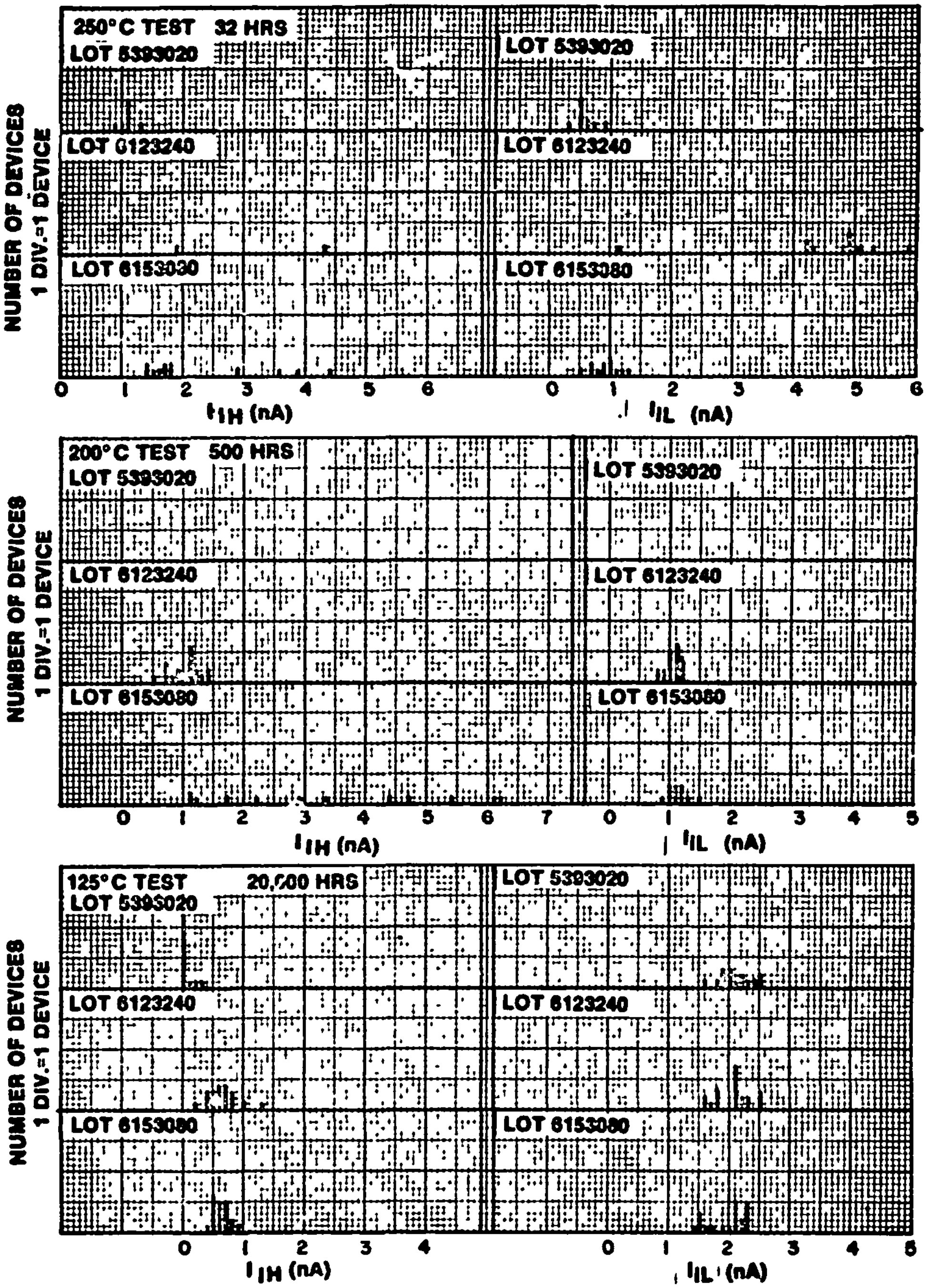
Distribution of ΔV_{OH} and ΔV_{OL} at V_{DD}=5V, T=125°C, for device type CD4011A.



Distribution of $\Delta V_{th}(P)$ and $\Delta V_{th}(N)$ for device type CD4011A.



Distribution of ΔI_{SS} at V_{DD}=15V, T=125°C, for device type CD4013A.



Distribution of I_{IL} and I_{IH} at V_{DD}=15V, T=125°C, for device type CD4013A.

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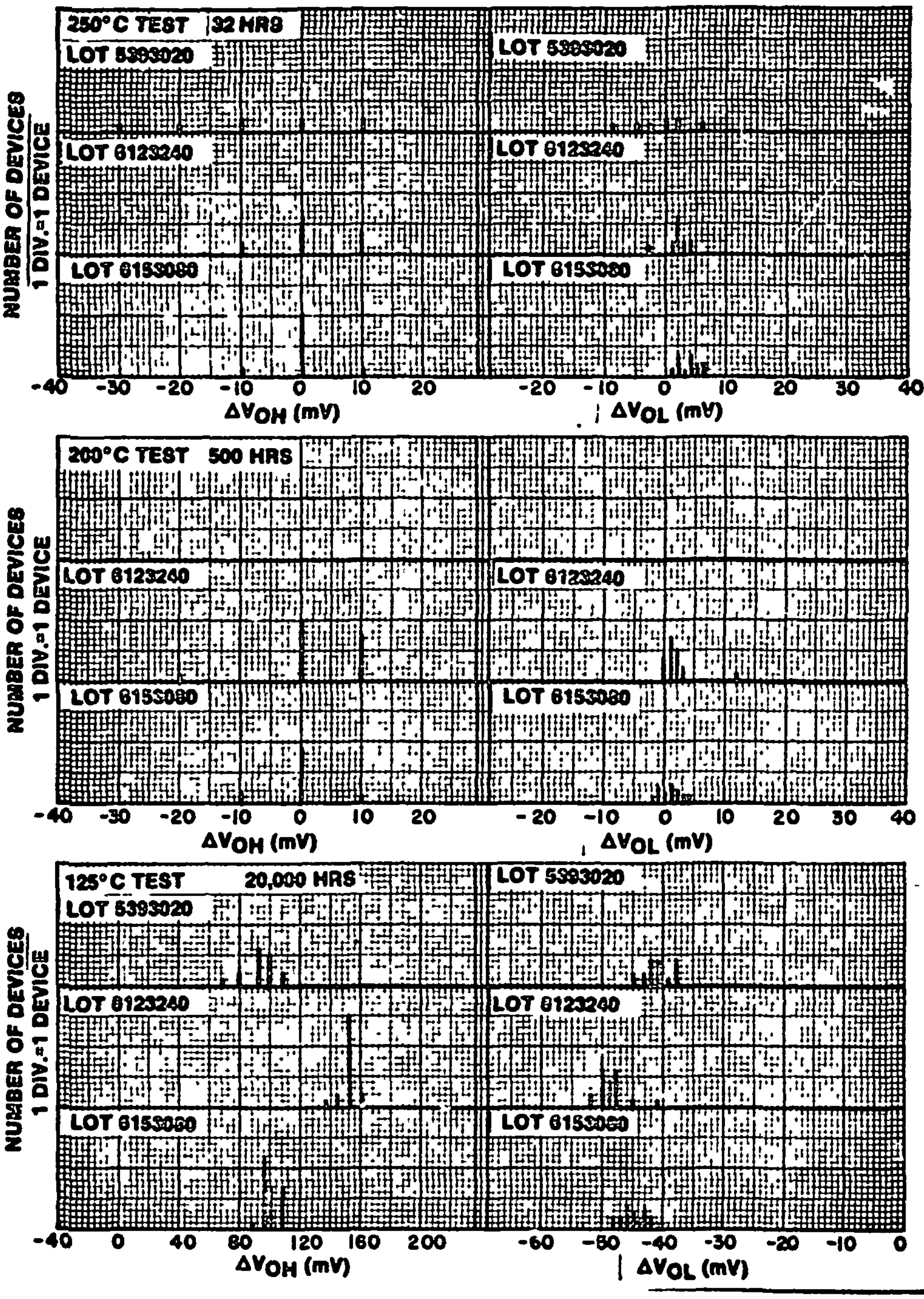
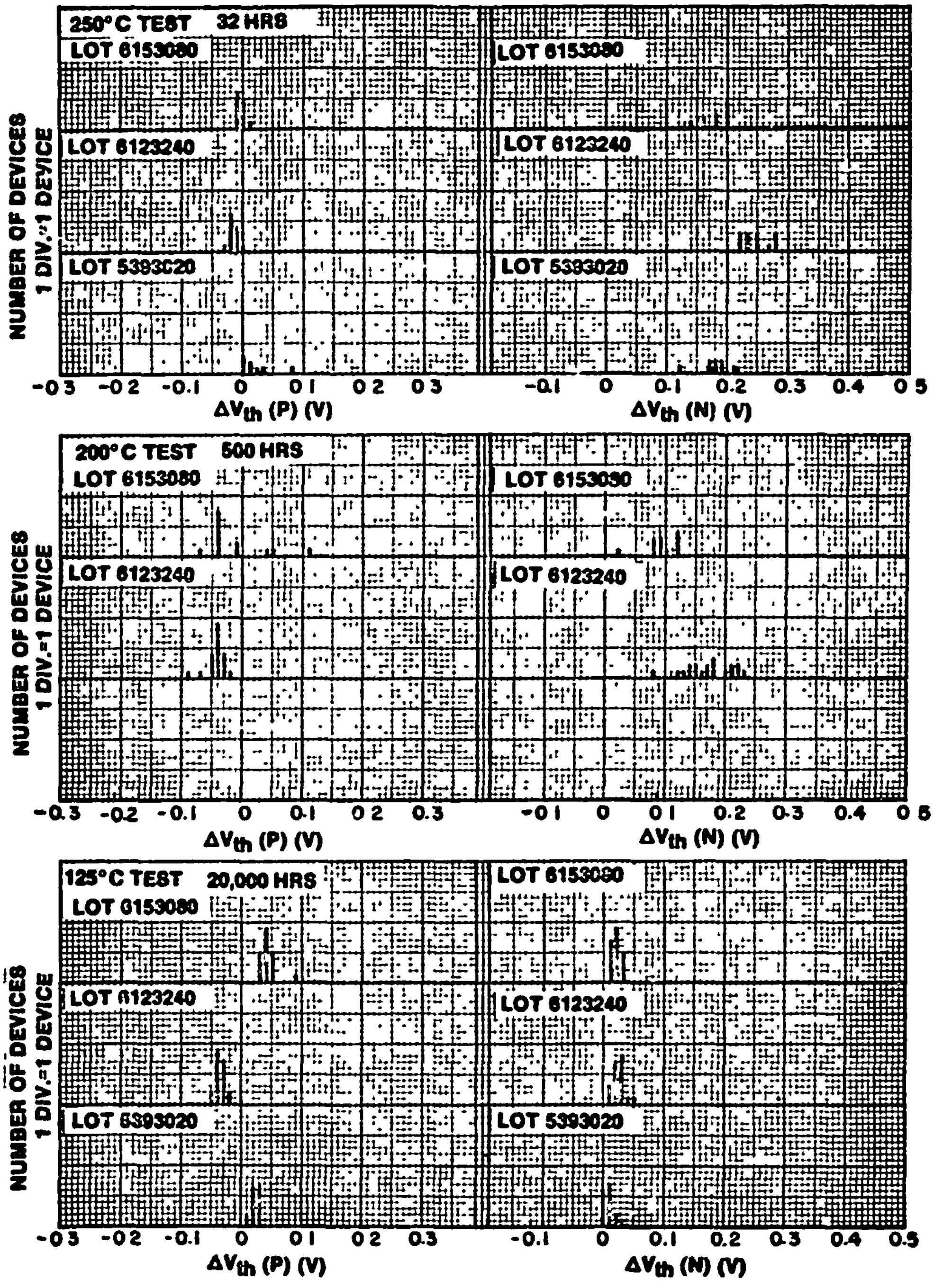
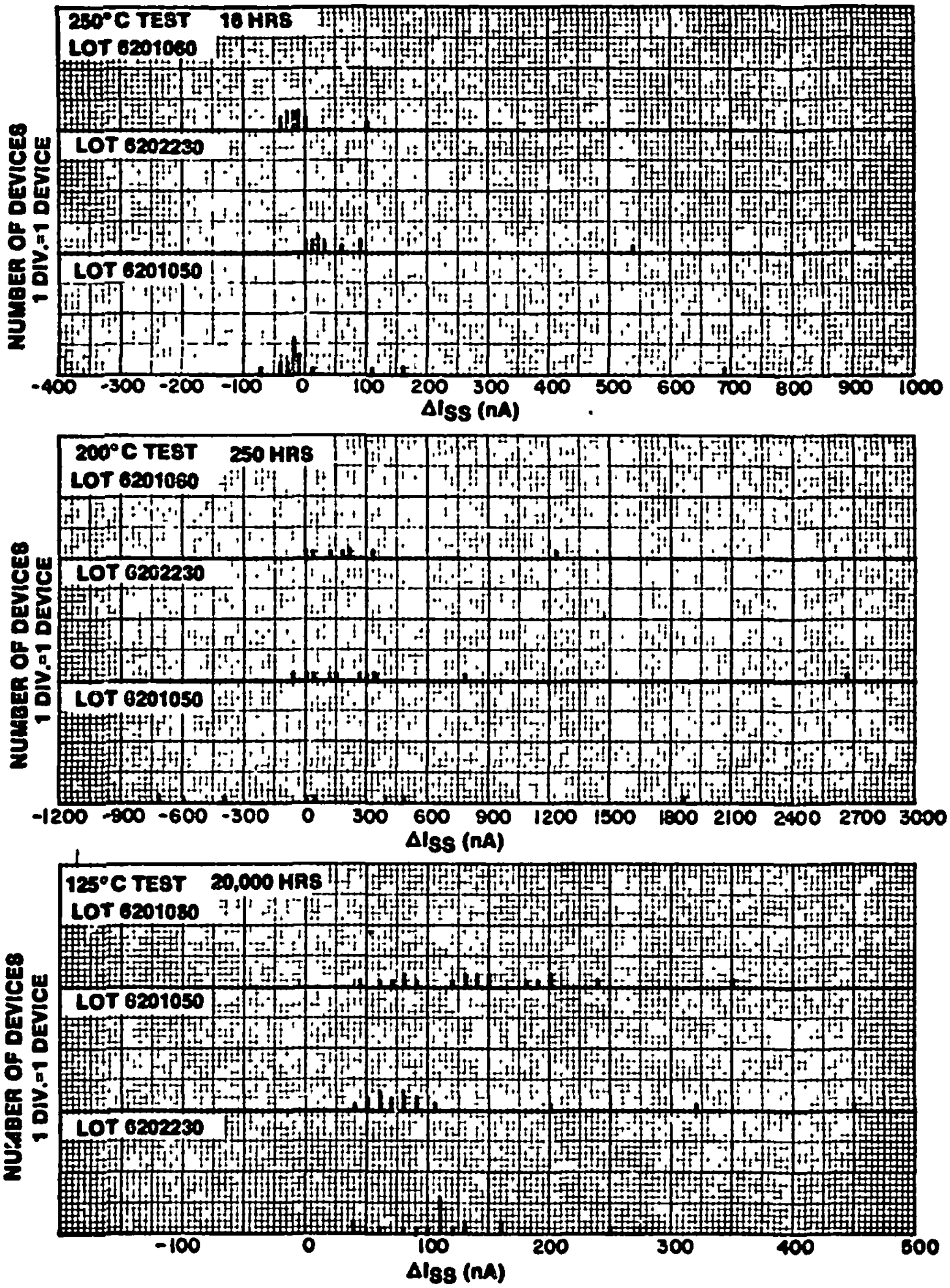


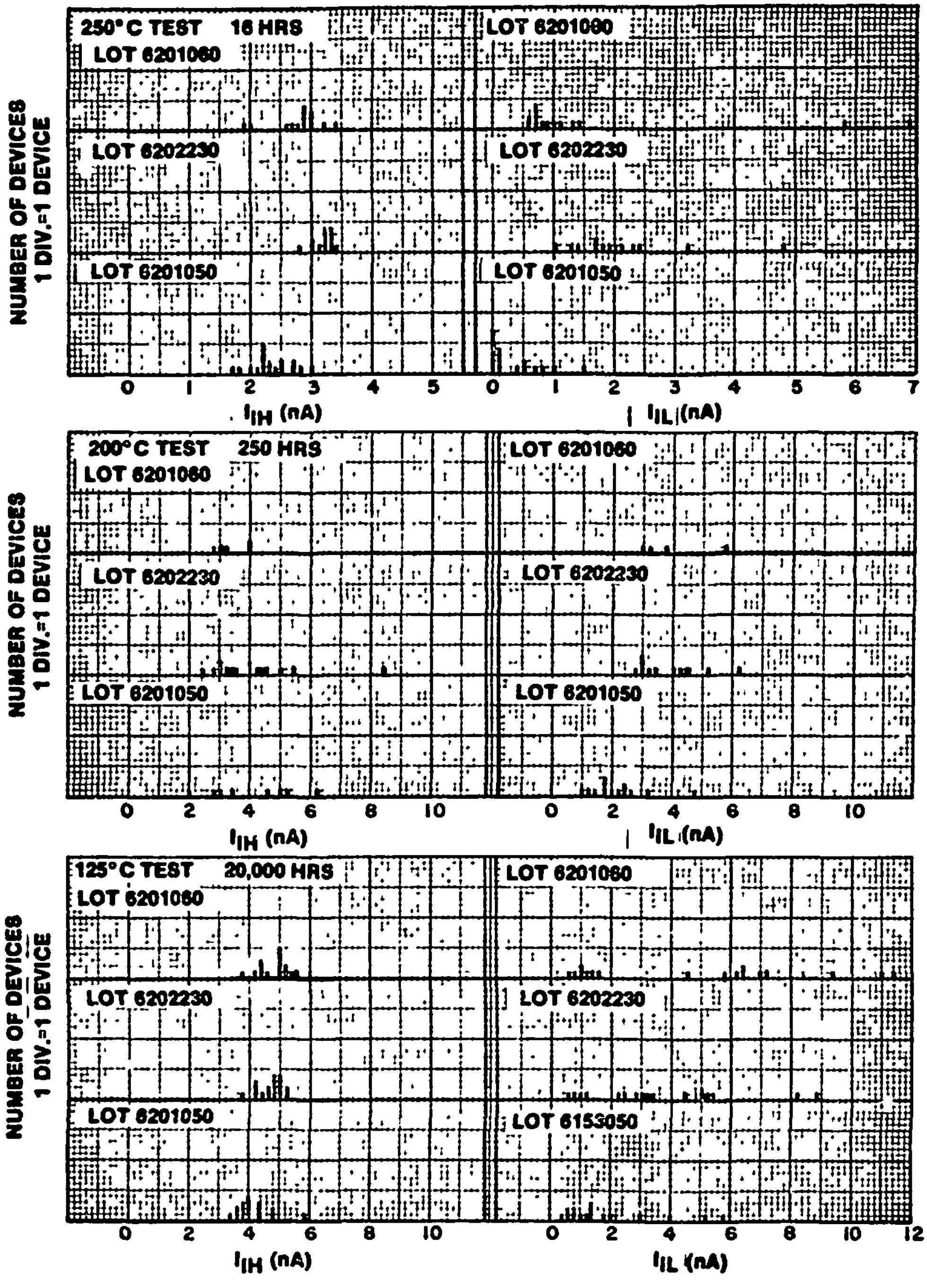
Distribution of ΔV_{OH} and ΔV_{OL} at V_{DD}= 5V, T=125°C, for device type CD4013A.



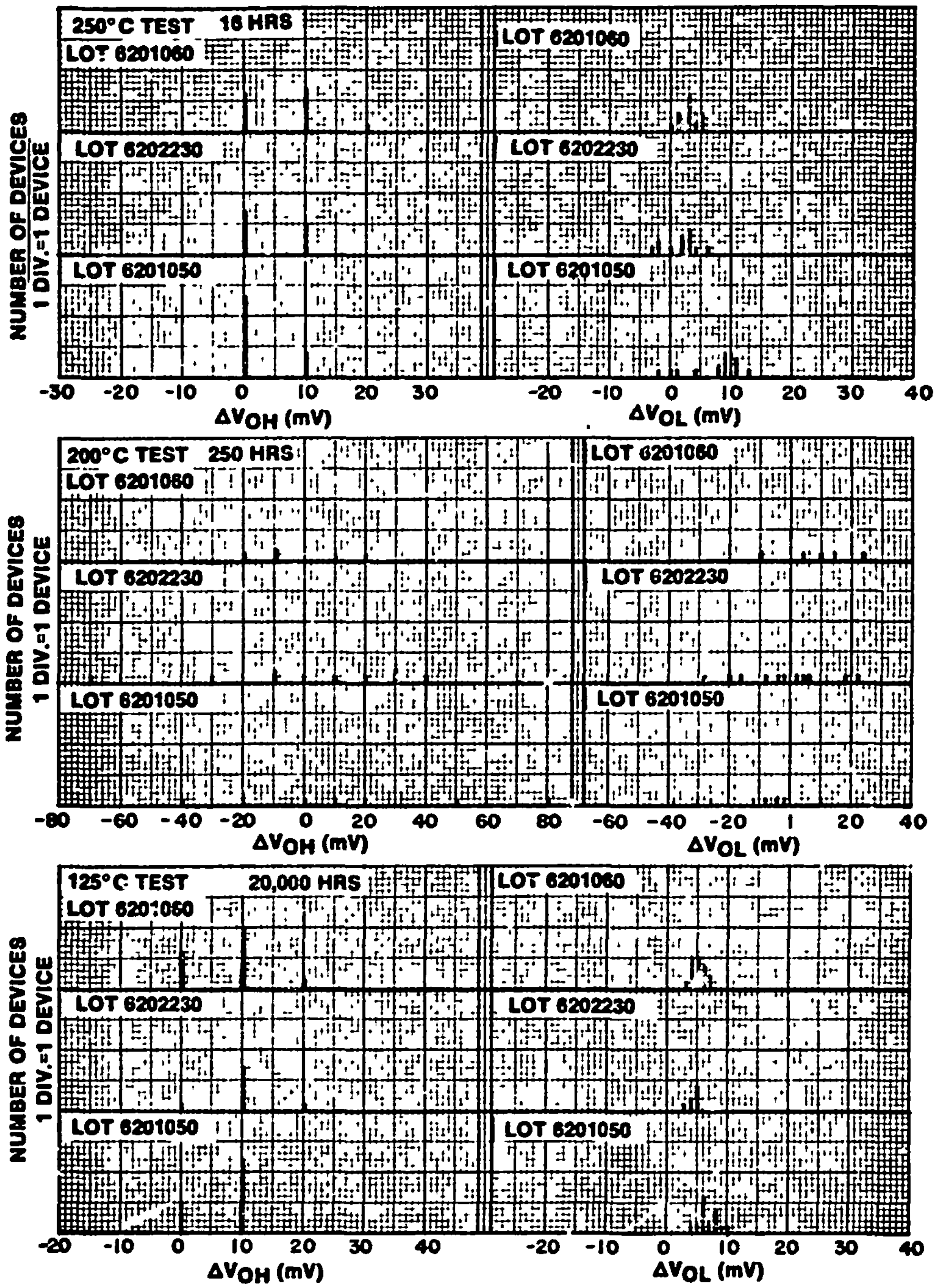
Distribution of $\Delta V_{th}(P)$ and $\Delta V_{th}(N)$ for device type CD4013A.



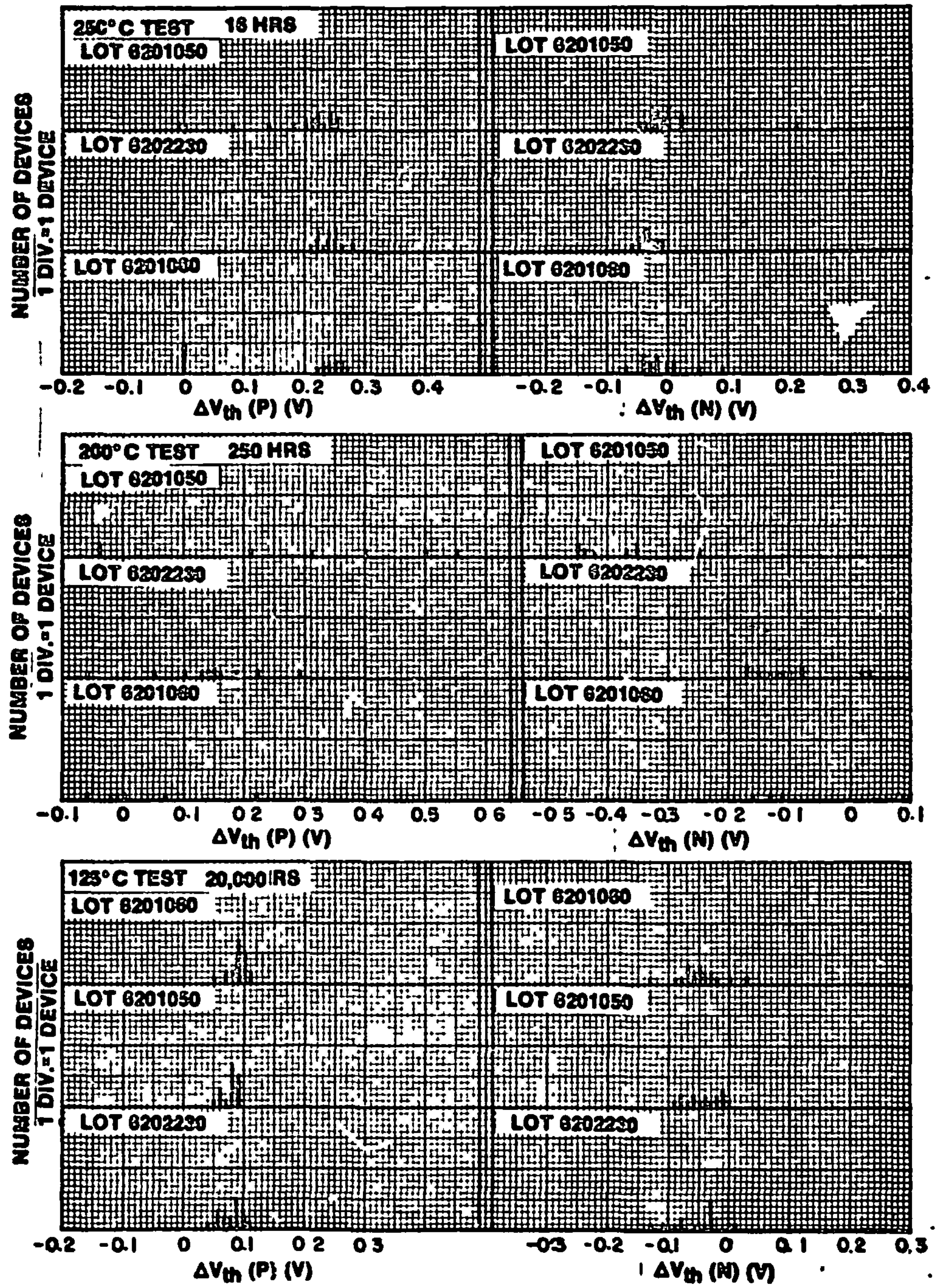
Distribution of ΔI_{SS} at V_{DD}=15V, T=125°C, for device type CD4024A.



Distribution of I_{IH} and I_{IL} at V_{DD}=15V, T=125°C, for device type CD4024A.



Distribution of ΔV_{OH} and ΔV_{OL} at V_{DD}=5V, T=125°C, for device type CD4024A.



Distribution of $\Delta V_{th}(P)$ and $\Delta V_{th}(N)$ for device type CD4024A.

There are three I_{SS} tests in the M38510/05001 (CD4011A) specifications. The results of all three of these tests were used in the parameter trend tables and graphs. From the M38510/05101 (CD4013A) and M38510/05605 (CD4024A) test results, three I_{SS} tests for each type were selected to avoid presentation of repetitious data. The selected I_{SS} test data indicated the greatest parameter shift. The leakage versus time plot indicates a fair stability for the surviving CD4011A, but shows considerable movement for the CD4013A and CD4024A. The 25°C measurements seems to track the 125°C measurements, indicating that for the purpose of observing leakage shift, both measurement temperatures are equally effective.

Improvement with the Bake

All failures from the 250°C test were subjected to a 200°C, 24-hour stabilizing bake. A large percentage of the failures showed improvement and some recovered completely. The results of this bake are tabulated in Table XXIII. These post bake results are the first indications that the instability of the CMOS microcircuits tested under the high-temperature accelerated conditions is possibly caused by the presence of mobile ions.

Gas Analysis

Prior to gas analysis, all test devices were subjected to a hermeticity test. All devices were hermetic. Twelve devices (four from each device type) were subjected to gas analysis. The devices were chosen to represent typical failures within each device type. Devices which did not fail were also included. The analysis on these twelve devices was performed by the RCA Methods and Materials Laboratory in Somerville. The summary of this analysis is given in Table XXIV. This table indicates the type of failure for each device: I_{SS} - total leakage, Ii - input leakage, F - functional failure, V_{th} - threshold failure. Although the threshold voltage is not identified as a test parameter by the MIL-M-38510 specifications, it was routinely measured at all measurement points. The threshold tests are included in the table as indicators of device stability under the accelerated testing, but are not considered as one of the criteria for failures.

TABLE XXIII

SUMMARY OF POST BAKE RESULTS

250°C Life Test
200°C 24 Hr Bake

Type/Lot	Hrs. L.T.	No. of Failures	Post Bake Improved Amt	Post Bake Improved %	Post Bake Recovered Amt	Post Bake Recovered %
CD4011A						
5361740	120	17	5	29	10	59
6153050	120	18	8	44	8	44
CD4013A						
5393020	32	11	3	27	7	64
6153080	64	19	8	42	7	37
6123240	32	10	1	10	8	80
CD4024A						
6201060	32	15	8	53	3	20
6202230	64	18	15	83	1	6
6201050	32	11	3	27	1	9

TABLE XXIV - Summary of Gas Analysis (RCA)[1]

Device Type	CD4011A				CD4013A				CD4024A			
Device Number	4	29	33	56	42	88	10	77	33	62	58	4
Type of Failure	Iss	Iss, V_{th}	Good	Good	Iss	Iss, I_{IL}/I_{IH} F, V_{th}	I_{IL} I_{IH}	I_{IL} I_{IH}	Iss, I_{IL} I_{IH}	Iss	Good	Iss
Post Bake Result / Constituent[2]	R	I	-	-	I	I	R	R	NI	NI	-	I
H_2 %	.15	-	.1	.17	.2	.11	-	.038	830 ppm	.12	.61	.08
He %	-	-	-	-	-	-	-	-	-	-	-	-
H_2O %	1.2	.15	.33	.06	.29	.47	-	-	.46	.34	.42	3.34
N_2 %	96.8	91.5	93.5	89.1	88.8	88.0	93.9	90.5	80.9	82.1	83.46	74.79
O_2 %	.16	.26	.32	.15	.22	.17	.18	.15	.17	.10	.1	.36
Ar %	-	-	.05	-	-	-	-	-	370 ppm	150 ppm	.37	.09
CO_2 %	.29	7.6	5.05	9.16	9.8	10.6	5.6	8.77	16.8	15.9	14.33	20.06
Propane %	.82	.16	-	-	.26	.29	-	-	.67	.58	-	-
Acetone %	-	.23	-	-	.31	.21	.44	.15	490 ppm	.42	.42	.38
Ethanol. %	750 ppm	.12	-	-	.15	.12	890 ppm	.4	680 ppm	660 ppm	.06	.08
Acetylene %	.47	-	-	-	-	-	-	-	.32	.27	-	-

Notes:
1. Symbols used in this table are defined in Table XXV, page 57.
2. All measurements shown are in percent by volume unless otherwise noted.

Devices which did not fail are identified with "good". The table further identifies devices which recovered after the bake with R, those which improved with I, and those that did not improve with NI. The constituent analysis is given in percent by volume unless otherwise indicated. In addition to the listed constituents, small amounts (not exceeding 500 ppm) of other organic compounds were found.

Twelve additional devices (four from each device type) were made available to Rome Air Development Center upon request by NASA so that the gas analysis could be performed by RADC. The summary of RADC findings is tabulated in Table XXV. The summary table has only two constituents shown (H_2O and CO_2), which appear to be the two most significant indicators. It can be seen that only those devices which were on the accelerated tests display considerable increase in the amount of H_2O and CO_2. The amount of water in the CD4011A and CD4013A but not in the CD4024A devices correlates (inversely) to time to failure. The CD4011A failures at the indicated time (64 and 32 hours) amounted to small increases of input leakage. Multiple failures were recorded at 120 hours. The CD4024A's (Nos. 42 and 30), although they had high water-vapor content, did not fail at 32 hours, and for that reason the time is indicated in parenthesis, but the test on the entire lot was discontinued, having accumulated at least 50-percent of failed devices.

It should be noted that there is significant difference in the amount of moisture indicated by the two gas analyses, one performed by RCA and the other by RADC. These variations are attributed to the differences in measurement techniques. RCA measurements are instantaneously done at room temperature; RADC measurements use integration techniques and are conducted at 100°C.

Chip Analysis

Representative failures from all three device types were opened and failure analysis performed. This analysis was aimed at determining the possible cause for the failures. The summary of this analysis is given in Tables XXVI through XXIX. The tables identify the devices, failure indicators, pins at which problems were detected, and the failure mechanisms.

TABLE XXV - Summary of Gas Analysis (RADC)

Device Type	CD4011A				CD4013A				CD4024A			
Device Number	49	50	39	41	23	24	94	95	42	30	19	20
Failure Indicator	C	C	I_{IL} I_{IH}	I_{II} I_{IH}	C	C	Iss, Vo F	Iss F, V_{th}	Good	Good	Iss	Iss, I_{IL} I_{IH} Vo
Time to Failure, Hrs.	-	-	64	32	-	-	64	16	(32)	(32)	32	64
Constituent / Post Bake Result	-	-	I	I	-	-	I	NI	-	-	I	NI
Water Vapor (%) Carbon Dioxide (%)	.1 .3	.1 .3	7.8 7.9	5.9 7.2	- .6	.1 .4	4.5 6.3	12.2 10.9	12.2 7.7	12.0 6.0	16.8 9.7	11.8 7.1

C = Control Device
F = Functionality
I = Improved
I_{IL}/I_{IH} = Input leakage
Iss = Total device leakage
NI = No improvement
R = Recovered after bake
Vo = Output voltage
V_{th} = Threshold voltage

TABLE XXVI - CD4011A Failure Analysis

250°C Test

Lot No. Device No.	Failure Indicator	Failure Mechanism and/or Cause
5361740 18	Iss, V_O, Lkg P4,7,10,11	P10 drain to source N channel - minor ionic contamination.
6153050 28	Iss, V, P13-P14 short, Lkg P3,4,7,10,11 - P2,6, 9,13 bias high	P13 - VDD diode shorted. SEM shows cracks at breakdown site. Electrical overstress.
6153050 36	Iss, V, Lkg P3,4,7,10	P channel MOS of P3,4,11 had inversion leakage in 50-100 nanoamp ~ange; baking @ 200°C did not improve. Etching oxide cleared leakage. Mobile ion contamination.
6153060 53, 54, 55	Pin 7 open	Vss metal run burned open. Latch during life.

I_{ss} - Leakage into V_{DD} pin.

V_O - Output voltage

Lkg - Leakage into other than V_{DD} pin

TABLE XXVII - CD4013A Failure Analysis

250°C Test

Lot No. Device No.	Failure Indicator	Failure Mechanism and/or Cause
6123240 7	Iss, Lkg 7,8,9	Leakage on P9 transmission gate to VDD = 100mA cleared with oxide etch. Mobile ion contamination.
6153080 89	-	Unit in carrier backwards.
6153080 90	Iss, V_{th}(P), Lkg, P1 2,7,12,13	Heavy invers. - 5uA plus, V_{DD} to Vss diodes cleared with aluminum etch, probably inversion where metal run was over oxide.

I_{ss} - Leakage into V_{DD} pin

V_o - Output voltage

Lkg - Leakage into other than V_{DD} pin

V_{th} - Threshold voltage

TABLE XXVIII - CD4024A Failure Analysis

$250^{o}C$ Test

Lot No. Device No.	Failure Indicator	Failure Mechanisms and/or Cause
6202230 2	Iss, V_o, $V_{th}(P)$, P14 Lkg. P3 Lkg with clock low = 130uA high = 10uA	P3 - V_{DD} diode. Leakage cleared with Al etch. P3 N&P MOS source to drain. Leakage cleared with Al etch + $200^{o}C$ bake 16 hr. Mobile ion contamination.
6202230 11	Iss, V_o, $V_{th}(P)$ Leakage P7,14, P3 lkg. during toggle switch	Vss to V_{DD} diode 1uA inversion leakage + 4V breakdown. Bake increased inversion to 2.5uA. Leakage cleared with oxide etch, Mobile ion contamination.
6201060 26	Iss, Lkg. P14 - Low Breakdown, 1.8V, P4,P5 Lkg during 10V pulse test.	P5, drain to source, N channel 10uA @ 20V cleared with bake. Mobile ion contamination.
6201060 27	Iss, Pulse test. P1 - IDD = 2.4mA	P1 and P2 P channel source to drain = 20uA. Inversion leakage cleared with $200^{o}C$ bake. Mobile ion contamination
6201050 51	Iss, V_o, $V_{th}(P)$, Lkg. P7, P14	Carrier insert had melted. Failure analysis halted.

I_{ss} - Leakage into V_{DD} pin

V_o - Output voltage

Lkg - Leakage into other than V_{DD} pins

V_{th} - Threshold voltage

TABLE XXIX - CD4013A Failure Analysis

200°C Test

Lot No. Device No.	Failure Indicator	Failure Mechanism and/or Cause
5393020 334	Continuity Fail. P1,P2 - Short P7 Open, P12,P13 - Short.	Multiple sites of large localized current between P2 and P12. Drains + Vss. Vss metal run burned open. Cause: Electrical overstress during life.
5393020 335	Same as 334	Same as 334
5393020 336	P2, P12 short. P7 Open	Same as 334

SECTION VIII

CONCLUSIONS

The results of accelerated testing of CMOS microcircuits which had been screened in accordance with Table II of MIL-M-38510 detail specification for class A devices, lead to the following conclusions:

1. The applicability of accelerated life tests at 250°C and 200°C as accurate predictors of CMOS device reliability at the use temperature of 125°C has not been experimentally verified because of insufficient data at 125°C after 20,000 hours of testing.

2. The 250°C test temperature is not practical because:
   a) Deterioration of devices at this temperature is too rapid to permit an accurate determination of the failure distributions under the real-life manufacturing environment.
   b) Test facilities are costly to maintain.
   c) Changes in materials used in test facilities at this temperature introduce errors and uncertainties that are impossible to control.

3. The "infant mortality" or "freak" distribution extends beyond 1000 hours in the 125°C accelerated tests. Therefore, the 1000-hour, 125°C life tests, as specified in MIL-M-38510 detail specifications, due to the combination of test conditions, the acceptance criteria, and the inadequacy of the burn-ins, tend to reject lots on the basis of the "infant mortality" failures. Under those circumstances it is a poor predictor of the reliability of CMOS microcircuit devices.

4. The complexity of the CMOS microcircuits has been observed to influence the time-to-failure of a device.

5. Leakage total (I_{SS}) and input (I_{IH}/I_{IL}) was the preponderant failure mode. Leakage failures recovered through baking.

6. Dependence of time-to-failure upon moisture content could not be verified.

7. The activation energies between 250°C and 200°C were estimated to be as follows: for CD4011A, 1.35eV; for CD4013A, 1.25eV; and for CD4024A, 1.0eV. Insufficicent data from the 125°C test cell prevented a more accurate three-point verification of these estimated activation energies.

8. Development of accelerated life-test specifications that could be equally effective in predicting reliability for all CMOS microcircuits could not be accomplished for the following reasons:
   a) Insufficient data at 125°C test temperatures.
   b) Varying complexity of devices apparently influenced the results of testing.
   c) Variation of the activation energy from device type to device type.

SECTION IX

RECOMMENDATIONS

On the basis of the test results and the conclusions reached, a program for the development of the accelerated life-test conditions can be recommended along the following guidelines:

Recommendations

It is essential for the development of the accelerated test specifications to establish correlation experimentally between the failure distributions at the use temperature (125°C) and the temperature to be used for the accelerated test. Testing beyond 20,000 hours at 125°C is, therefore, recommended. Should the failure distributions at 125°C correlate with those at 200°C, a two-test-point specification to control both the freak and the main distributions ought to be considered. Should the failure distributions be significantly different from those at 200°C, other test temperatures between 125°C and 200°C must be investigated.

The relationships between the complexity of microcircuits and their reliability needs to be investigated in more detail. Various life-test conditions may be required, based on microcircuit complexity groups. As the complexity of a microcircuit increases, there is less certainty as to the state in which a complex device finds itself when fixed bias is used. Therefore, dynamic versus fixed bias-life test conditions need to be explored. The use of non-burned-in devices in life testing investigations should be helpful in assessing the effectiveness of burn-ins in removing freak distributions. The present limits for input leakage (1 nA for an individual input pin) at downtime measurements in life testing should be relaxed in order to overcome mild instabilities that may occur in the device, in the environment, or in the testing system. A 10X initial limit is suggested for the individual input pins and a 5X initial limit is suggested for the ganged input-pin measurements.

APPENDIX A

ACCELERATED LIFE TESTING EFFECTS ON CMOS MICROCIRCUIT CHARACTERISTICS

Selection of an optimum deposition and combination of protective layers through testing and evaluation of Silicon Nitrite (SiN_4)

Phase IV Report

November 1977 to April 1979

June 1979

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ACCELERATED LIFE TESTING EFFECTS ON
CMOS MICROCIRCUIT CHARACTERISTICS

PHASE IV REPORT

CONTRACT NAS8-31905

I. INTRODUCTION

The results of Phase I and Phase II of this contract (250°C and 200°C accelerated tests) as well as work done by RCA's various activities in the field of reliability improvement suggest that reduced longevity of the CMOS microcircuits under high-temperature accelerated testing is primarily due to contaminants external to the chip. The presence of small amounts of moisture enhances the mobility of the contaminant ions, thereby contributing to increased leakage currents and changes in other device characteristics, such as threshold and output voltage, under the high-temperature accelerated testing. Phase IV introduces modifications and additions to the present process of making CMOS microcircuits which are designed to provide protective layers on the chip to guard against moisture and contaminants.

II. OBJECTIVES

1. The improvement of the Class A CMOS microcircuit high-temperature accelerated-test characteristics through deposition of silicon nitride protect layers.
2. The selection of the optimum process for further evaluation under high-temperature accelerated-test conditions.

III. THE PROCESS

The standard wafer-manufacturing process was modified by the introduction of two distinctly different silicon nitride (Si_3N_4) protect layers. These two kinds of Si_3N_4 layers are distinguished by the method of deposition and, therefore, resultant characteristics.

The high-temperature Si_3N_4 layer is deposited in a furnace at 800°C. This method of deposition results in a dense layer which is impervious to contaminants, has a slow etch rate, and which provides a good barrier to sodium. The deposition of the layer over the field oxide presents few problems. When the layer is deposited over the channel oxide, its thickness must be minimized (175 - 200Å) to prevent the formation of a metal-to-channel oxide interface and the possibility of accumulation of undesirable charges. Fig. 1(c) shows the location of this layer.

The low temperature Si_3N_4 layer is plasma deposited after the metallization, at 310°C, a temperature low enough to prevent alloying of aluminum metal into the silicon. This type of deposition results in a less dense layer with a higher etch rate. The layer is deposited over the entire chip and is made relatively thick (3kÅ to 10kÅ) in an attempt to make it impervious to contaminants, Figs. 1(b) and (c). The PSG (phosphorous silica glass) layer standard in current RCA processing is retained with the idea that it may still serve the useful function of gettering for those contaminants that might be trapped under the protect layer.

VI. DEVICE SELECTION

The simplicity of the CD4007A device type was the compelling reason for choosing it as the vehicle for this experiment. A wealth of life-test information is also available for this device type. The schematic diagram of Fig. 2 shows the internal connections of the CD4007A; the easy accessability to individual transistors should greatly facilitate the analysis of failures resulting from subsequent testing and evaluation.

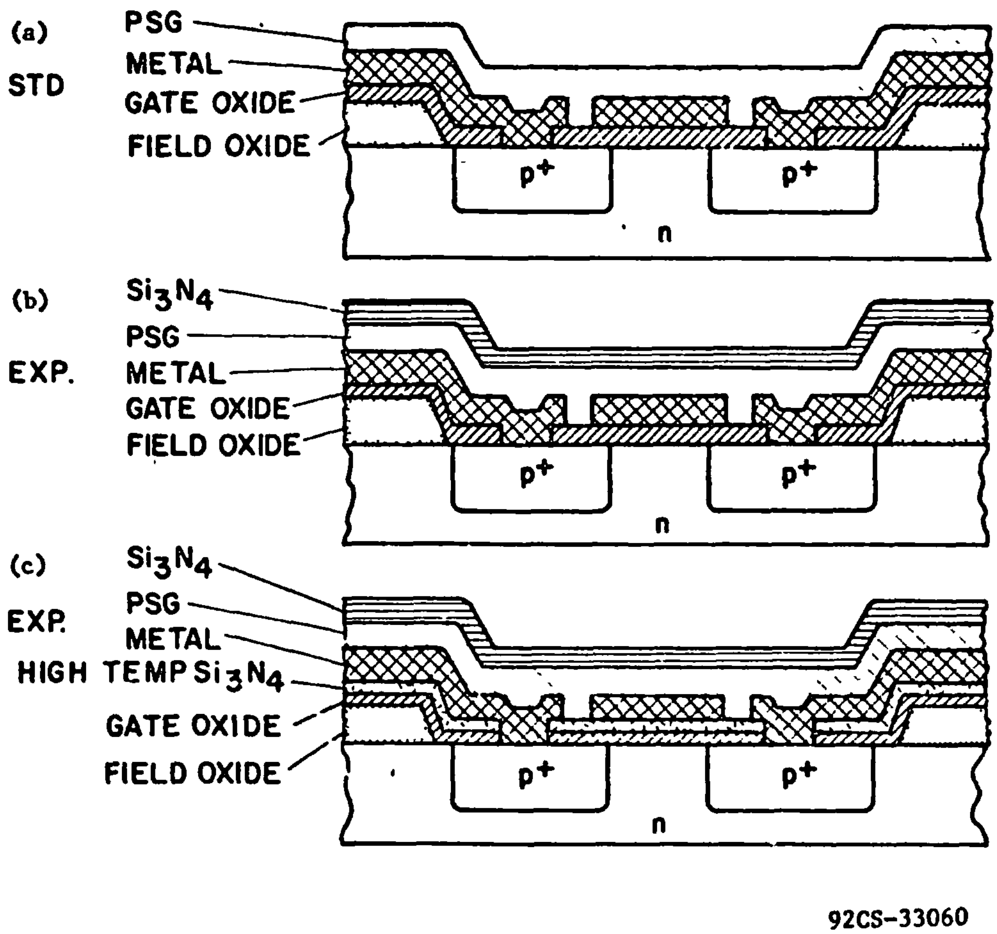


Fig. 1 - Deposition of layers on p-channel transistor.

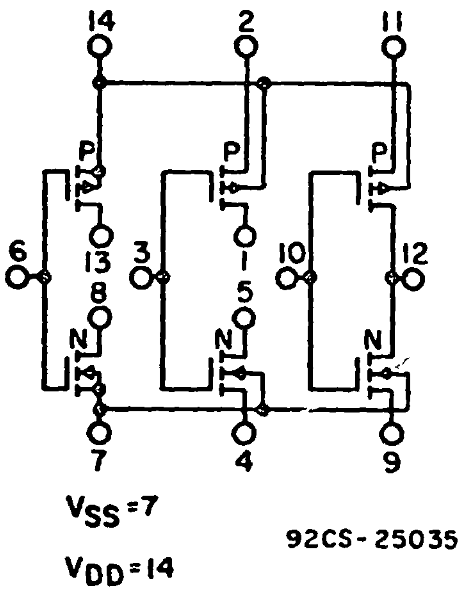


Fig. 2 - Schematic diagram for CD4007A. Dual complementary pair plus inverter.

V. DEVICE FABRICATION

The experimental cell matrix was developed as shown in Fig. 3. Twenty-four wafers were processed by means of the standard RCA process for fabricating commercial CMOS IC's through channel-oxide deposition. At this point, the wafer lot was divided into two parts. One half received a deposition of high temperature Si_3N_4 over the field and the gate oxides. Then the entire lot was put through standard processing up to the final step of low-temperature Si_3N_4 deposition. At this step, eight cells (1 through 8) were created on which the low temperature Si_3N_4 was deposited in various thicknesses. Cell No. 1 was designated as the control cell and received no Si_3N_4 deposition. Cells No. 2, 3, and 4 had only the low temperature Si_3N_4 deposited. Cell No. 5 had the high temperature Si_3N_4 only. Cells No. 6, 7, and 8 had both the high temperature and the low temperature Si_3N_4 deposition. After the wafer processing had been completed, cells No. 1, 4, and 10 were further divided, so that one half of each could be assembled with eutectic mounts in ceramic packages. Consequently cells No. 9, 10, and 11 are eutectically mounted devices from cells No. 1, 4 and 8, respectively.

The wafers were circuit probed with high resultant yields, which is a good indicator of the manufacturability of the process. For comparison, the circuit probe yields for the CD4007A were:

For the 1977 year, 80 to 85%
For the Si_3N_4 experiment, 82%

The control cell (No. 1) and the test cells (Nos. 2 through 8) were assembled in standard plastic dual-in-line packages. The pellets were mounted with epoxy used in the RCA CD4000 commercial series. The Novolac plastic package is thought to accentuate problems that might be encountered in subsequent testing, thereby reducing the duration of tests. The assembled devices were screened to commercial specifications to net 60 good devices per cell for further evaluation.

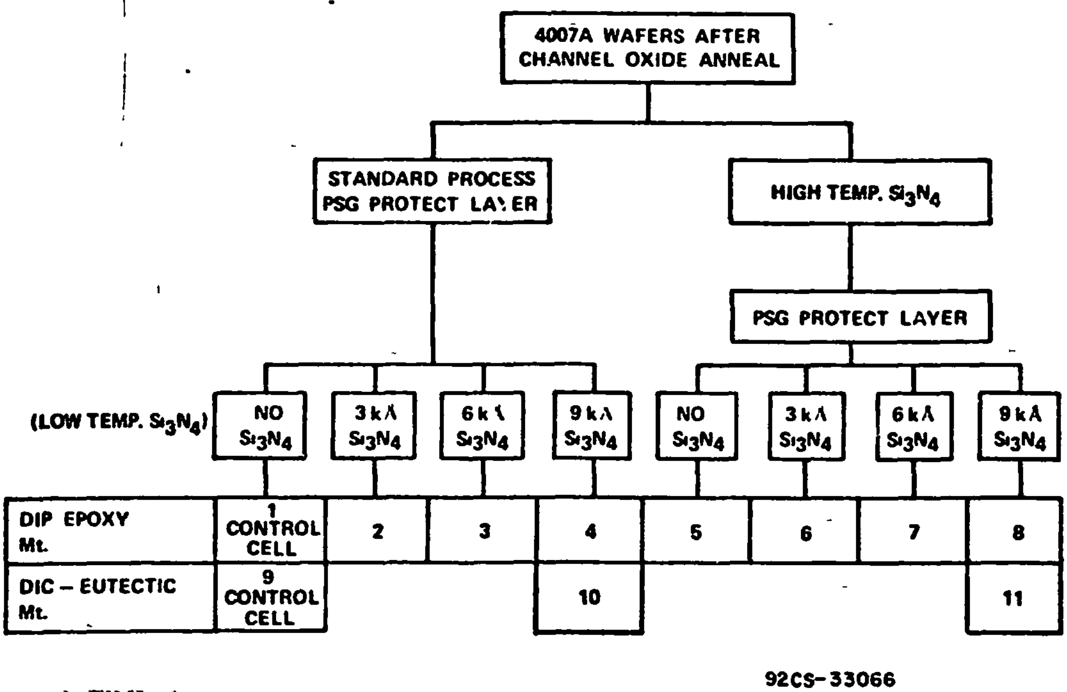


Fig. 3 - Experimental cell matrix.

The devices in test cells Nos. 9, 10 and 11 were to be eutectically mounted in ceramic (DIC) packages so that they could be tested under high-temperature accelerated-test conditions. These three cells represent those test cells appearing as the last line in the experiment matrix of Fig. 3.

VI. TEST AND EVALUATION

The evaluation of the effectiveness of the Si_3N_4 protect layers as the barriers to contaminants required the type of testing that provides sufficient stressing, particularly in two areas: the high-temperature and high-humidity environment. Three tests were used to achieve this type of stress:

1. 200°C bias/temperature test
2. 150°C bias/temperature test
3. 85°C/85% relative-humidity, bias/humidity tests.

All tests were conducted at 12.5 V dc. The circuit bias arrangement used was the standard burn-in bias configuration shown in Fig. 4. Each test cell from No. 1 to No. 8 was tested in accordance with the schedule of Fig. 5. The electrical measurements were taken initially and at each down-time as indicated for tests 1, 2, and 3. The anticipated end-of-test time for each test is also shown in Fig. 5 as the last down-time.

It was thought, from experience, that all test cells would have generated a sufficient number of out-of-specification devices at each end-of-test time to provide the basis for comparison among the test cells. However, it was found during the actual testing that the longevity of the test devices was underestimated. Neither 240 hours at 200°C nor 1152 hours at 150°C were producing enough out-of-specification devices for conclusive evaluation. Because of time and equipment limitations it was then decided to continue beyond the anticipated end-of-test time with the 200°C bias-temperature test only. The 200°C test in actuality had to be extended to 500 hours and eventually to 768 hours before a conclusive evaluation could be done.

The test parameters and the limits used in testing cells 1 through 8 were those of the standard commercial device specifications. The use of specifications more relaxed than those of the MIL-M-38510 detail specifications was dictated by the need to detect gross differences among the test cells rather than differences resulting from subtle process variations. Table I gives the commercial specification test limits.

One group of devices, Cells 9, 10 and 11 were designated to be tested to MIL-M-38510 detail specifications, Table II. These devices were assembled in ceramic packages with eutectic mounts and tested with a 200°C bias/temperature test so that the test results could be compared to those obtained in Phase II. These devices were represented by the

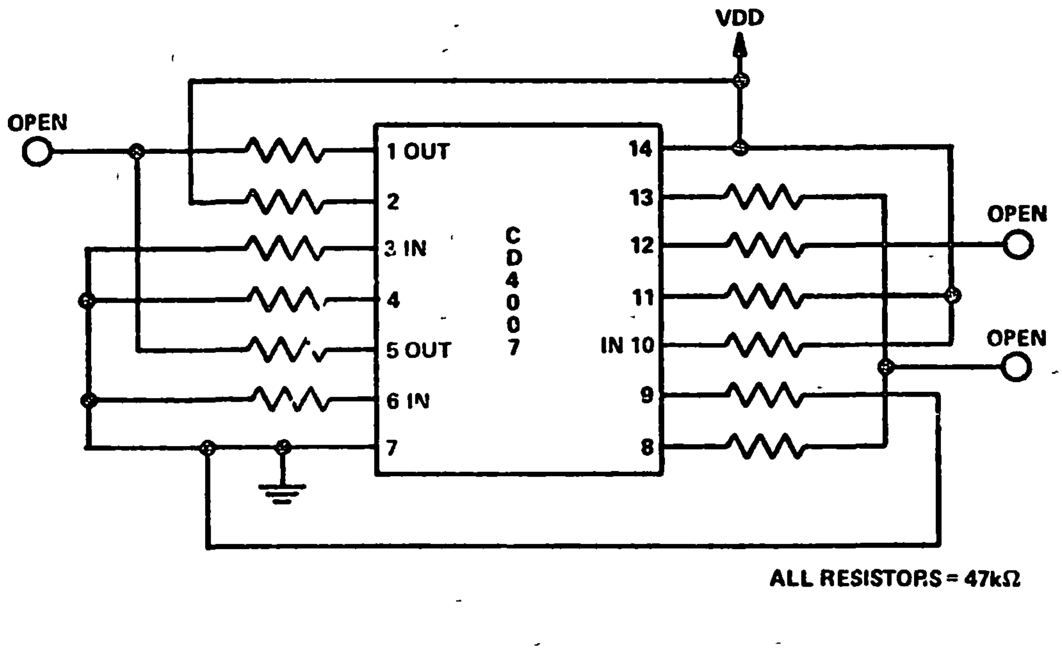
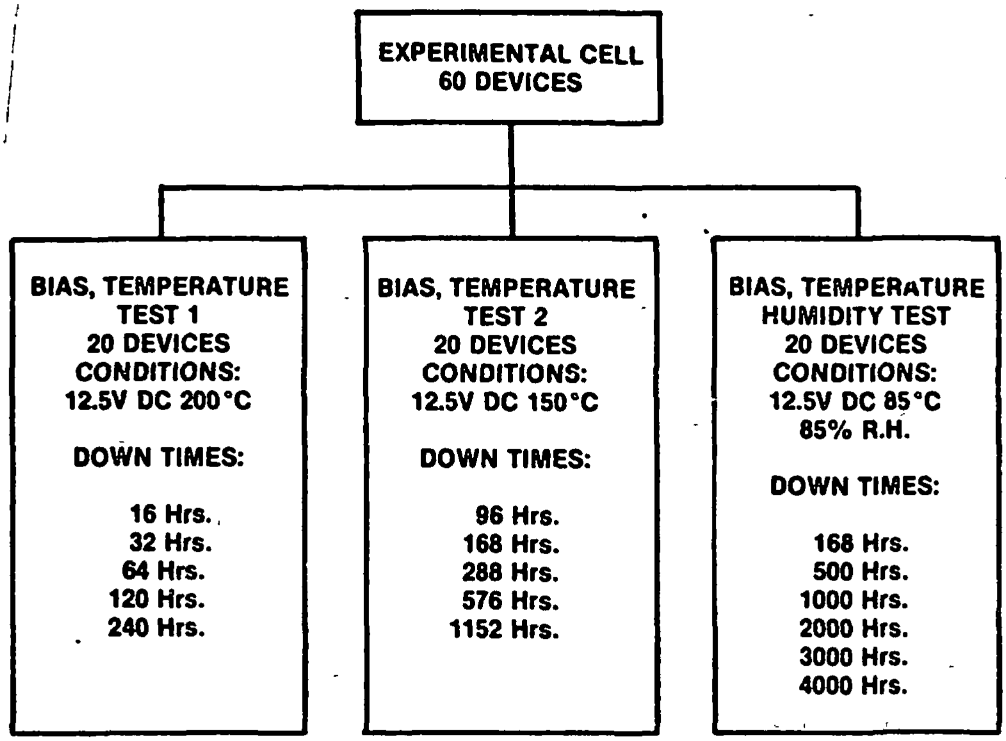


Fig. 4 - Burn-in diagram.



ALL DEVICES AT EACH DOWN-TIME ARE CRITICIZED TO COMMERCIAL LIMITS

Fig. 5 - Testing and evaluation of each cell.

TABLE I - Commercial Specification Test Limits

Parameter	Test Condition	Limits min.	Limits max.
Quiescent device current, I_L	V_{DD} = 10V		[illegible] mA
Qutput voltage, low level, V_{OL}	V_{DD} = 10V		0.01V
Output voltage, high level, V_{OH}	V_{DD} = 10V	9.99V	
Noise immunity	V_{DD} = 10V		
Low V_{NL}	V_o = 7.2V	3V	
High V_{NH}	V_o = 2.9V	3V	
Output drive current	V_{DD} = 10V		
n-channel I_{DN}	V_i=V_{DD}, V_o=0.5	1 mA	
p-channel I_{DP}	V_i =V_{SS}, V_o=9.5	-0.55 mA	

three test cells Nos. 9, 10, and 11. Test-cell No. 10 had the low temperature Si_3N_4 layer only while test-cell No. 11 had both the low-temperature and the high-temperature Si_3N_4 layers. Test cell No. 9 was accidentally lost during handling.

The electrical measurements on this group of devices were performed by using the test programs based on the MIL-M-38510 detail specifications. This method of testing provided test results directly comparable to earlier accelerated-test evaluations of CMOS microcircuits to the MIL-M-38510 specifications. It also provided a preview of the capability of the eutectic-mount and Si_3N_4 protect-layer combination under high-temperature accelerated-test conditions.

VII TEST RESULTS

The test matrix in this experiment was designed so that the analysis of the test results could be conducted in steps. At first a determination must be made as to whether there is an improvement in either of the two test groups over the control cell. If there is an improvement in more than one cell, a comparative evaluation among the test cells must be made to determine which of the test cells possesses the best characteristics. The improvement must be demonstrated in both the high-temperature and high-humidity environments. The test results are summarized in Table III.

The 150°C bias/temperature test can be eliminated from consideration immediately because the control cell has not produced a single out-of-specification device in this test. The results of the other two tests, the 200°C bias/temperature and the 85°C/85% relative-humidity tests, can be analysed by the application of the three regions in the life of a device: The "infant-mortality" region, the "constant-failure-rate" region, and the "wear-out" region.

None of the test devices has been burned-in; consequently, the devices which exceeded the specification limits during the first 16 hours in the 200°C test as well as the out-of-specification devices occurring within the first 168 hours in the 85°C/85% relative-humidity test could be attributed to the infant mortality. The constant-failure-rate region appears to fall between the 16-hour point and the 500-hour point in the 200°C test. At the 500-hour point, devices begin exceeding the specification limits in numerous cells,

TABLE II - Device CD4007A, MIL-M-38510 Detail Specification, Electrical Test Parameters

TABLE III. Group A inspection for device type 01.

Symbol	MIL-STD-883 method	Case A, C, D	Terminal conditions and limits															Test limits						Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Subgroup 1 $T_A = 25°C$		Subgroup 2 $T_A = 125°C$		Subgroup 3 $T_A = -55°C$		
		Test No	2aY	2as	2A	2bs	2bY	1A	V_{SS}	1bY	3bs	3A	3as	3Y	1aY	V_{DD}		Min	Max	Min	Max	Min	Max	
V_{IC} (POS)		1	(5)	GND			(1)	1 mA		(13)			GND		(8)	GND	1A		1.5					Vdc
V_{IC} (POS)		2		GND	1 mA								GND			GND	2A		1.5					
V_{IC} (POS)		3		GND								1 mA	GND			GND	3A		1.5					
V_{IC} (NEG)		4				GND		-1 mA	GND		GND						1A		-6					
V_{IC} (NEG)		5			-1 mA												2A		-6					
V_{IC} (NEG)		6										-1 mA					3A		-6					
I_{SS}	3005	7		15 V	GND			GND				GND	15 V			15 V	V_{SS}		-50		-500			nA
I_{SS}	3005	8		15 V	15 V			15 V				15 V	15 V			15 V	V_{SS}		-50		-500			nA
V_{OH1}	3006	9		4.5 V	GND			V_{IL1}				GND	4.5 V		I_{OH1}	4.5 V	1aY	2.5		2.5		2.5		Vdc
V_{OH1}		10	I_{OH1}	4.5 V	V_{IL1}			GND				GND	4.5 V			4.5 V	2aY	2.5		2.5		2.5		
V_{OH1}		11		4.5 V	GND			GND				V_{IL1}	4.5 V	I_{OH1}		4.5 V	3Y	2.5		2.5		2.5		
V_{OH2}		12		5.0 V	GND			V_{IL1}				GND	5.0 V		I_{OH2}	5.0 V	1aY	4.5		4.5		4.5		
V_{OH2}		13	I_{OH2}		V_{IL1}			GND				GND					2aY	4.5		4.5		4.5		
V_{OH2}		14			GND			GND				V_{IL1}		I_{OH2}			3Y	4.5		4.5		4.5		
V_{OH3}		15			GND			V_{IL1}				GND					1aY	4.95		4.95		4.95		
V_{OH3}		16			V_{IL1}			GND				GND					2aY	4.95		4.95		4.95		
V_{OH3}		17			GND			GND				V_{IL1}					3Y	4.95		4.95		4.95		
V_{OH4}		18		12.5 V	GND			V_{IL2}				GND	12.5 V			12.5 V	1aY	11.25		11.25		11.25		
V_{OH4}		19		12.5 V	V_{IL2}			GND				GND	12.5 V			12.5 V	2aY	11.25		11.25		11.25		
V_{OH4}		20		12.5 V	GND			GND				V_{IL2}	12.5 V			12.5 V	3Y	11.25		11.25		11.25		
V_{OL1}	3007	21		5.5 V	GND			V_{IH1}				GND	5.5 V		I_{OL1}	5.5 V	1aY		0.4		0.5		0.4	
V_{OL1}		22	I_{OL1}	5.5 V	V_{IH1}			GND				GND	5.5 V			5.5 V	2aY		0.4		0.5		0.4	
V_{OL1}		23		5.5 V	GND			GND				V_{IH1}	5.5 V	I_{OL1}		5.5 V	3Y		0.4		0.5		0.4	
V_{OL2}		24		5.0 V	GND			V_{IH1}				GND	5.0 V		I_{OL2}	5.0 V	1aY		0.5		0.5		0.5	
V_{OL2}		25	I_{OL2}		V_{IH1}			GND				GND					2aY		0.5		0.5		0.5	
V_{OL2}		26			GND			GND				V_{IH1}		I_{OL2}			3Y		0.5		0.5		0.5	
V_{OL3}		27			GND			V_{IH1}				GND					1aY		50		50		50	mVdc
V_{OL3}		28			V_{IH1}			GND				GND					2aY		50		50		50	mVdc
V_{OL3}		29			GND			GND				V_{IH1}					3Y		50		50		50	mVdc
V_{OL4}		30		12.5 V	GND			V_{IH2}				GND	12.5 V			12.5 V	1aY		1.25		1.25		1.25	Vdc
V_{OL4}		31		12.5 V	V_{IH2}			GND				GND	12.5 V			12.5 V	2aY		1.25		1.25		1.25	Vdc
V_{OL4}		32		12.5 V	GND			GND				V_{IH2}	12.5 V			12.5 V	3Y		1.25		1.25		1.25	Vdc
I_{IH1}*		33		15 V	15 V			15 V				15 V	15 V			15 V	All inputs together		3.0					nA
I_{IH2}		34		15 V	GND			15 V				GND					1A		1.0		45			
I_{IH2}		35		15 V	15 V			GND				GND					2A				45			
I_{IH2}		36		15 V	GND			GND				15 V					3A				45			
I_{IL1}*	3009	37		15 V	GND			GND				GND					All inputs together		-3.0					
I_{IL2}		38		15 V	15 V			GND				15 V					1A		1.0		-45			
I_{IL2}		39		15 V	GND			15 V				15 V					2A				-45			
I_{IL2}		40		15 V	15 V			15 V				GND					3A				-45			
C_i	3012	41		GND		GND		K	GND		GND		GND			GND	1A		12					pF
C_i		42			K												2A		12					pF
C_i		43										K					3A		12					pF

See notes at end of device type 01.

TABLE II (continued)

TABLE III. Group A inspection for device type 01 - Continued.

Symbol	MIL-STD-883 method	Case A, C, D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Meas. terminal	Subgroup 9 $T_A = 25°C$		Subgroup 10 $T_A = 125°C$		Subgroup 11 $T_A = -55°C$		Unit
		Test No.	2aY	2as	2A	2bs	2bY	1A	V_{SS}	1bY	3bs	3A	3as	3Y	1aY	V_{DD}		Min	Max	Min	Max	Min	Max	
t_{PLH}	3003 (Fig 8)	44	(5)	5 0 V	GND	GND	(1)	IN	GND	(13)	GND	GND	5 0 V		(8)	5 0 V	1A to 1aY		110		165		110	ns
t_{PLH}		45			IN			GND				GND					2A to 2aY		.10		165		110	
t_{PLH}		46			GND			GND				IN					3A to 3Y		110		165		110	
t_{PHL}		47			GND			IN				GND					1A to 1aY		170		255		170	
t_{PHL}		48			IN			GND				GND					2A to 2aY		170		255		170	
t_{PHL}		49			GND			GND				IN					3A to 3aY		170		255		170	
t_{THL}	3004 (Fig 8)	50			GND			IN				GND					1aY		240		300		240	
t_{THL}		51			IN			GND				GND					2aY		240		360		240	
t_{THL}		52			GND			GND				IN					3Y		240		360		240	
t_{TLH}		53			GND			IN				GND					1aY		160		240		160	
t_{TLH}		54			IN			GND				GND					2aY		160		240		160	
t_{TLH}		55			GND			GND				IN					3Y		160		240		160	

NOTES

A Pins not designated may be "high" level logic, "low" level logic or open Exceptions are as follows: $V_{IC(POS)}$ tests, the V_{SS} terminal shall be open; $V_{IC(NEG)}$ tests, the V_{DD} terminal shall be open, I_{SS} tests, the outputs shall be open.

B. I_{OH1} = -0 1 mA at 25°C, -0 1 mA at 125°C; -0 1 mA at -55°C.

C. I_{OH2} = -0.30 mA at 25°C, -0 21 mA at 125°C, -0.375 mA at -55°C

D. V_{IH1} = 3 95 V at 25°C, 3 85 V at 125°C, 4 05 V at -55°C.

E. V_{IH2} = 10 25 V at 25°C, 10 0 V at 125°C, 10 5 V at -55°C

F. I_{OL1} = .23 mA at 25°C, .4? mA at 125°C, 23 mA at -55°C.

G. I_{OL2} = 600µA at 25°C, 400 µA at 125°C; 750 µA at -55°C.

H. V_{IL1} = 0.9 V at 25°C, 0 65 V at 125°C, 0 95 V at -55°C

I V_{IL2} = 2 25 at 25°C, 1 95 V at 125°C, 2.40 V at -55°C.

J Terminals in parentheses are connected together as indicated by the included number.

K. See 4 4.1(c).

L * Indicates the device manufacturer may, at his option, measure I_{IL} and I_{IH} at 25°C for each individual input or measure all inputs together.

TABLE III - Test Result of Cells No. 1 Through 8; Number of Out-of-Specification Devices

Test Description	Cell No.	Standard Process With Low Temp. Si_3N_4				High Temp. Si_3N_4 Layer With Low Temp. Si_3N_4			
	Cell No.	1	2	3	4	5	6	7	8
	Si_3N_4 Thickness	0A	3kA	6kA	9kA	0A	3kA	6kA	9kA
	Sample Size	20	20	20	18	20	20	20	19
	Downtime Hours								
200°C Bias/Temperature Test	16	0	0	0	2	0	0	0	0
	32	0	0	0	0	0	0	0	0
	64	0	0	2	0	0	0	0	0
	120	0	0	1	0	0	0	0	1
	240	0	0	0	0	0	0	0	0
	500	1	0	4	0	8	0	5	3
	768	14	18	10	16	12	17	12	12
	Cumulative	15	18	17	18	20	17	17	16
	Sample Size	20	20	20	20	18	19	16	20
	Downtime Hours								
150°C Bias/Temperature Test	96	0	0	0	0	1	1	2	0
	168	0	0	0	0	0	0	0	0
	288	0	1	0	0	0	0	0	0
	576	0	0	1	0	0	0	1	0
	1152	0	0	1	0	0	0	0	0
	Cumulative	0	1	2	0	1	1	3	0
	Sample Size	19	20	20	20	19	20	18	20
	Downtime Hours								
85°C/85% R.H. Bias/Humidity Test	168	1	0	0	0	0	0	0	0
	500	0	0	0	0	1	0	0	0
	1000	0	0	1	0	0	0	0	0
	2000	0	2	0	0	2	0	0	0
	3000	0	1	0	0	3	1	2	3
	4000	5	7	1	1	1	6	0	1
	Cumulative	6	10	2	1	7	7	2	4

C-2

an indication of the onset of the wear-out region. The test data at 768 hours clearly indicates that the wear-out region for all the cells has been reached before that time. Because of the absence of out-of-specification devices in the control cell within the constant-failure-rate region, the wear-out region must be used as the criterion for comparative evaluation of cells. By using that criterion, cells 2, 4, and 6 appear as having demonstrated characteristics equal to or better than those of the control cell. None of these cells has had an out-of-specification device in the constant-failure-rate region, up to and including the 500-hour point. The two out-of-specification devices in cell No. 4 are attributed to infant mortality. The control cell had an out-of-specification device at the 500-hour point. The wear-out region for these test cells lies somewhere between 500 hours and 768 hours. The rate of deterioration for the devices in this region is probably similar for all cells, as can be judged by the recorded number of out-of-specification devices at the 768-hour point.

Similarly, the onset of the wear-out region in the 85°C/85% relative-humidity test, at least for some cells, is evidenced at the 4000-hour point. From among the test cells identified earlier, only cell No. 4 remains in the contest with the control cell because of the condition that a cell must demonstrate improvement in both the 200°C and 85°C/85% relative-humidity test to be in contention. At the 4000-hour point cell No. 4 has had one out-of-specification device versus five such devices (exclusive of one early out-of-specification device) in the control cell. This result tends to indicate the possibility that the heavy coat (9kÅ) of low-temperature Si_3N_4 is presenting a barrier to moisture. The group with two Si_3N_4 layers did not do as well, in general, suggesting that perhaps the technique of depositing the thin high-temperature Si_3N_4 layer may need further perfecting.

Test cells No. 10 and 11 were tested at 200°C and evaluated to the MIL-M-38510 detail specifications. At the 16-hour down time, both test cells had produced devices out of specification in leakage (I_{SS}); test cell No. 11 has had devices with out-of-specification leakage (I_{SS}), and with p-threshold voltage deteriorating to 0.5 to 0.9-volt levels. One device had zero p-threshold voltage at the 16-hour test point.

Table IV summarizes the number and kind of out-of-specification devices which occurred in test cells No. 10 and 11. The threshold problems have occurred in the same devices that failed leakage tests. The early problems of the kind that were observed indicated the possible presence of mobile ions. This possibility was checked in both test cells by baking devices at 150°C for 24 hours. A complete recovery in some cases and partial recovery in many others was observed. The bias/temperature test was repeated for another 16 hours, and a recurrence of excessive I_{SS} and V_{TH} problems was observed. The threshold deterioration in test cell No. 11, which has both Si_3N_4 layers, is further evidence of the presence of mobile ions in the lot with the high temperature Si_3N_4 layer. The results of this testing do not compare favorably with the results of tests conducted in Phase II of this contract on CD4011A, CD4013A, and CD4024A devices. Due to a large number of failures (40% in one cell and 75% in the other) the test was terminated after 16 hours of testing.

CONCLUSION

The results of the evaluation of the high-temperature and low-temperature Si_3N_4 protect layers conducted within the scope of this effort lead to the following conclusions:

1. The application of the Si_3N_4 layers in all of the tested combinations failed to lead to a demonstrably conclusive improvement in device reliability characteristics.

2. There is some evidence that a heavy (9kÅ) layer of low-temperature Si_3N_4 presents a barrier to moisture. A further, more detailed study is required for a more conclusive statement.

3. The testing of eutectically mounted devices has not produced a desirable degree of improvement in reliability characteristics.

TABLE IV - Test Results for Eutectically Mounted CD4007A, Cells 10 and 11

200°C Bias/Temperature Test

Cell No.	10	11
Sample size	20	20
No. of failures at 16 hours	8	15
Type of failures	I_{SS}	I_{SS} ($V_{th(n)}$, 9 devices)*

*For information only

MIL-M-38510 detail specification does not criticize for V_{th}. Nine devices had $V_{th(n)} < 1.0V$.

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